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Poly-4-vinylphenol and poly(melamine-co-formaldehyde)-based graphene passivation method for flexible, wearable and transparent electronics

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Next generation graphene-based electronics essentially need a dielectric layer with several requirements such as high flexibility, high transparency, and low process temperature. Here, we propose and investigate a flexible and transparent poly-4-vinylphenol and poly(melamine-co-formaldehyde) (PVP/PMF) insulating layer to achieve intrinsic graphene and an excellent gate dielectric layer at sub 200 °C. Chemical and electrical effects of PVP/PMF layer on graphene as well as its dielectric property are systematically investigated through various measurements by adjusting the ratio of PVP to PMF and annealing temperature. The optimized PVP/PMF insulating layer not only removes the native –OH functional groups which work as electron-withdrawing agents on graphene (Dirac point close to zero) but also shows an excellent dielectric property (low hysteresis voltage). Finally, a flexible, wearable, and transparent (95.8%) graphene transistor with Dirac point close to zero is demonstrated on polyethylene terephthalate (PET) substrate by exploiting PVP/PMF layer which can be scaled down to 20 nm.

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1. Introduction

Next generation flexible, wearable, and transparent electronics (FWTEs) such as electronic-paper, wearable display, flexible touch screen, and transparent wall, are expected to be mechanically flexible, optically transparent, and light in weight.^{1–4} For the transistors that these devices are fundamentally composed of, novel materials such as indium tin oxide (ITO), zinc tin oxide (ZTO), carbon nano tube (CNT), and polyimide have been previously proposed as electrode, active channel, and dielectric layers.^{5–10} Although zero band gap graphene is limited in the present situation for complementary metal–oxide–semiconductor (CMOS) applications due to its low on/off-current ratio and high power consumption, it is still a promising candidate for FWTEs because of its high mobility ($\sim 200\,000\text{ cm}^2\text{ V s}^{-1}$), flexibility (fracture strain of 30%), and

transparency (97.5% for monolayer).^{11–14} However, two critical issues need to be resolved before utilizing graphene as a FWTEs material; finding a flexible and transparent insulator for gate dielectric and maintaining its intrinsic electrical property.

Recently, 2D dielectrics such as boron nitride (BN) and mica have been applied for graphene-based devices because of low roughness, reduction of interfacial carrier scattering, and better scale-down potential for future devices.¹⁵ However, it is still a challenge to achieve large area BN and mica-based devices are incompatible with flexible electronics. Another insulating materials such as ion gel, high-k dielectric, and graphite oxide (GO) have been also studied for the graphene-based FWTEs.^{16–19} Even though these insulators show good electrical combination with graphene, high cost of raw materials for ion gel, non-uniformity of the GO layer, and high thermal processing of high-k dielectric layer are hindering the successful integration of graphene-based FWTEs. In addition, it is a challenging task to achieve graphene layers with intrinsic property where the concentration of holes and electrons are symmetric. The root of these issues lies in the unexpected doping problem on graphene surface caused by native hydroxyl (–OH) functional groups under atmospheric ambient and polymer-residues deposited during the fabrication process.^{20–26} Because the p-type doping problem degrades the performance of graphene-based devices, several methods such as encapsulation by BN, vacuum anneal, and chemical cleaning process, have been proposed to remove

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the unexpected $-OH$ groups and polymer-residues on the graphene surface.^{27–29} However, these methods are not suitable for FWTE technology because their processing temperature exceeds 200 °C where most flexible substrate is bound to melt and the interaction problem that exists between the chemical solution and the flexible substrate. Although a clean-lifting process through electrostatic generator which can provide a polymer-residue free graphene on flexible substrates has been reported recently,³⁰ it does not seem to be free from the p-type doping problem by native $-OH$ functional group formation. In this letter, we propose and investigate a poly-4-vinylphenol and poly(melamine-co-formaldehyde) (PVP/PMF)-based insulating layer to obtain a transparent and flexible gate dielectric layer on graphene and achieve and maintain intrinsic property of graphene at sub 200 °C. PVP/PMF-based insulator is a popular material for flexible and transparent organic electronics that can be easily formed by spinning-coating process and can also be scaled down by adjusting PVP/PMF concentration in PGMEA solution at sub 200 °C. In addition, the problematic $-OH$ groups on native graphene can be effectively combined with PMF cross-linking agent while PVP/PMF insulator fabrication. Based on these findings, a flexible and transparent graphene-based transistor with Dirac point close to zero is fabricated to demonstrate the feasibility of PVP/PMF-based insulator on graphene-based FWTEs. Even though various polymer dielectrics, such as polyimide and PMMA, were previously used on graphene-based flexible devices,^{31,32} the surface passivation phenomenon by the dielectric on graphene has not been reported yet.

2. Experimental details

2.1 Preparation of PVP/PMF solution

The 0.5 g of PVP was mixed with 4.5 g, 4.25 g, and 4 g of PGMEA to produce PVP solutions. Then, a different amount of PMF (0 g, 0.25 g, and 0.5 g) is added to these PVP solutions, yielding different PVP/PMF solutions which were respectively named as PVP/PMF 0%, 50%, and 100%.

2.2 Fabrication of graphene transistor

The graphene was synthesized on copper foil by conventional chemical vapor deposition (CVD) method.³³ The graphene/Cu foil was etched in ferric chloride ($FeCl_3$) and was transferred onto 300 nm thick silicon-dioxide (SiO_2) on heavily n-doped Si substrate. The transferred graphene was patterned by optical lithography and oxygen (O_2) plasma etching processes was used to define the active channel region of 8 μm of width and 80 μm of length. Finally, Ti (10 nm) and Au (50 nm) layers were deposited to form source/drain (S/D) metal electrodes by electron-beam evaporator.

2.3 Fabrication of PVP/PMF-based capacitor

The PVP/PMF 50% layer was spin-coated on p-type Si substrate, followed by 100 °C, 150 °C, and 200 °C anneal for 30 minutes to induce sufficient cross-linking process. Then, 100 nm thick Ni was deposited through a shadow metal mask with a square

pattern of 100 μm by 100 μm to form metal electrodes. Finally, metal (Ni)-insulator (PVP/PMF)-semiconductor (Si) structure based capacitor was fabricated.

2.4 Fabrication of transparent, flexible and wearable graphene electronics

First of all, the bottom dielectric layer was spin-coated on polyethylene terephthalate (PET) substrate using the optimized PVP/PMF 50% solution, followed by curing process at 150 °C. After transferring graphene on PVP/PMF, we selectively deposited Ti/Au layers by a lift-off process to form S/D regions and then patterned an active graphene channel region. Then, the PVP/PMF layer was spin-coated and other patterned Ti/Au layers were deposited to make a gate stack. For wearable graphene device, graphene-PVP/PMF layers were first deposited on polyvinyl alcohol (PVA)/Si substrate and a top gate transistor fabrication process on the sample was performed. Finally, the fabricated transistor device was floated on deionized (DI) water to transfer onto arbitrary places (researcher's finger in this paper).

3. Result and discussion

3.1 Raman spectroscopy analysis for PVP/PMF dielectric layer

First, the chemical properties of PVP/PMF are investigated in order to study the cross-linking interaction between PVP and PMF. PVP/PMF solutions were spin-coated on n-type silicon (Si) substrates and were annealed at 100 °C, 150 °C, and 200 °C. Then, Fourier transform-infrared spectroscopy (FT-IR) measurement was performed on the samples to analyze $-OH$ groups in the PVP/PMF layers. Fig. 1a–c show the spectra for

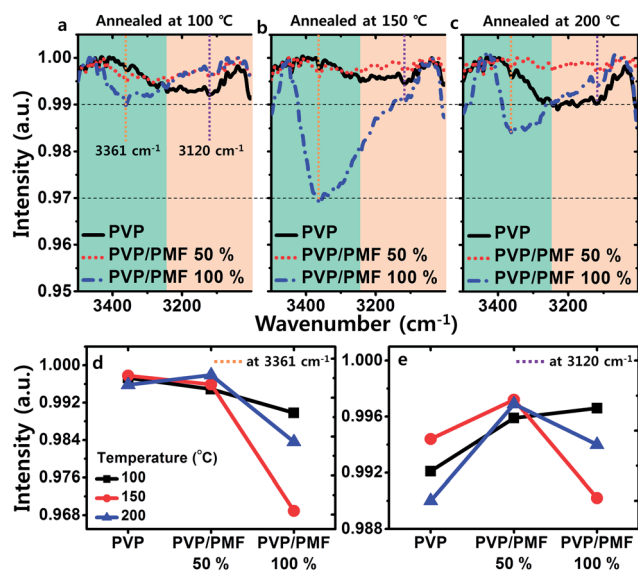


Fig. 1 Chemical analysis of PVP/PMF dielectric layers. FT-IR spectra of pure PVP, PVP/PMF 50%, and PVP/PMF 100% films annealed at (a) 100 °C, (b) 150 °C, and (c) 200 °C. Comparison of the extracted peak intensities for $-OH$ groups at (d) 3361 cm^{-1} and (e) 3120 cm^{-1} .

–OH groups in PVP/PMF layers, which are typically located between 3000 cm^{-1} and 3400 cm^{-1} . In the pure PVP sample without PMF, we found that the peak for –OH groups was around 3000 cm^{-1} to 3250 cm^{-1} . However, other peaks relating to –OH groups in PVP/PMF 50% and PVP/PMF 100% samples were observed at 3250 cm^{-1} to 3450 cm^{-1} . The reason for the different peak positions is related to the cross-linking mechanism between PVP and PMF, which makes PVP molecules to bond with PMF through –OH and –OH bonding during the annealing process, thereby reducing the number of –OH groups in PVP. As a result, –OH groups in the pure PVP and PVP/PMF films are respectively in non-hydrogen and hydrogen bonding states.²⁹ The difference of bonding states makes the peaks to be located at the slightly different positions. In the case of PVP/PMF 50%, as shown in Fig. 1d and e, very low and stable peak intensities were observed at all annealing temperatures compared to the PVP/PMF 100% sample, indicating that a proper concentration of PMF was mixed to cross-link with the –OH groups in PVP. It is predicted that high and unstable intensities of PVP/PMF 100% sample is attributed to the remaining –OH groups of PMF remaining after the cross-linking process.

3.2 Electrical analysis for PVP/PMF dielectric deposited graphene transistor with different PMF concentration

The PVP/PMF cross-linking process was then applied on the graphene surface by depositing and annealing PVP/PMF layers. Fig. 2a shows the schematic diagram of the fabricated graphene transistor and possible chemical reactions among –OH groups in graphene, PVP, and PMF. As widely known, native –OH groups are easily formed on graphene surface under

atmospheric condition, making the graphene layer to work as p-type materials.²³ Although there was an experimental report that the type of graphene converts to intrinsic through vacuum annealing process at $200\text{ }^{\circ}\text{C}$, very high positive Dirac point value ($\sim 50\text{ V}$) was still obtained in the graphene sample annealed at $200\text{ }^{\circ}\text{C}$ meaning that the graphene is still strong p-type.²⁸ However, in the graphene transistors with PVP, PVP/PMF 50%, and PVP/PMF 100% layers, Dirac points were respectively shifted to 27 V , 6 V , and -2 V after the $200\text{ }^{\circ}\text{C}$ anneal. It is thought that –OH groups in PVP and PVP/PMF are bonded with those on graphene surface during the annealing process, thus reducing the number of –OH groups on graphene. It seems that this effect is stronger as the PMF concentration increases in PVP solution. This observation suggests that the cross-linking process with –OH groups on graphene by PMF is expected to be more favorable than that by PVP at $200\text{ }^{\circ}\text{C}$. In order to re-verify the shifting of Dirac point according to different concentration of PMF, drain current–gate voltage (I_D – V_G) measurement and Dirac point extraction were performed on ten different graphene transistor devices, as shown in Fig. 2b and c. Here, it is confirmed that PVP/PMF layer can effectively reduce the number of –OH groups on graphene surface through the annealing process and PVP/PMF 50% is optimal in obtaining the intrinsic property of graphene with Dirac point at $\sim 0\text{ V}$ and working properly as an insulating material. Higher concentration of PMF to PVP is also expected to cause slight n-type doping phenomenon (consequently, negative Dirac point) on graphene due to the triazine structure with N atoms in PMF.³⁴

3.3 Raman analysis for graphene on PVP/PMF dielectric layer

Next, in order to investigate the change of graphene electronic structure according to the interaction between PVP/PMF and graphene, Raman spectroscopy ($\lambda = 532\text{ nm}$) was performed on graphene layers transferred on various bottom films, such as SiO_2 , PVP/PMF 50%, and PVP/PMF 100%, which were annealed at $200\text{ }^{\circ}\text{C}$ for 1 hour. Fig. 3a shows the Raman spectra measured on the graphene layers, where we observed conventional graphene D-, G-, D', and 2D peaks at around 1350 cm^{-1} , 1590 cm^{-1} , 1618 cm^{-1} , and 2683 cm^{-1} , respectively. As shown in Fig. 3b, D' peak appeared at 1618 cm^{-1} near G peak only in the graphene layers passivated by PVP/PMF 50% and 100% films. The newly appeared D' peaks in graphene samples reacted with PVP/PMF 50% and 100% layers can be explained by graphene structure modification through cross-linked –OH bonding and N atom doping phenomena between graphene and PVP/PMF layers. Yung-Chang Lin *et al.* and Zhiqiang Luo *et al.* also observed the D' peak in doped graphene layers and explained that it is attributed to the structural change of graphene surface by doping process.^{35,36} In addition, the three graphene samples (pristine, PVP/PMF 50%, and PVP/PMF 100%) show different positions of G and 2D peaks in Fig. 3c. In the case of pristine graphene sample, its G peak appeared at around 1597 cm^{-1} which is a slightly up-shifted value from that of intrinsic graphene ($\sim 1584\text{ cm}^{-1}$), confirming its p-type property that was previously concluded by I_D – V_G measurement. However, after

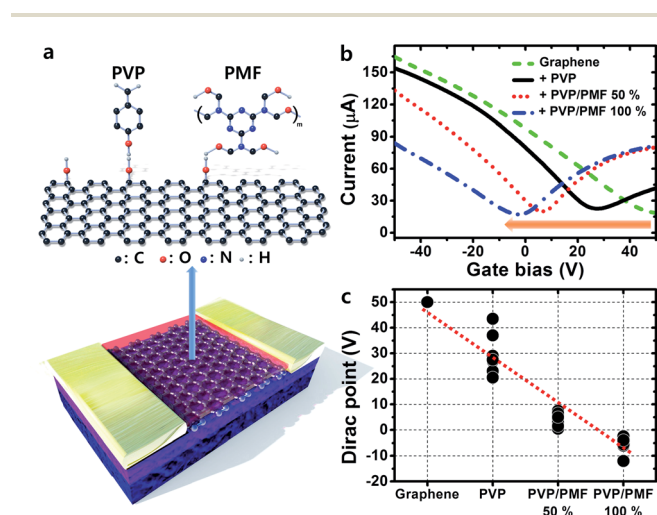


Fig. 2 Schematic diagram for possible chemical interactions and carrier transporting properties of graphene devices passivated by PVP/PMF with different PMF concentrations. (a) Schematic diagrams of fabricated graphene transistor, indicating chemical reactions by PVP and PMF on graphene. (b) I_D – V_G characteristics of graphene transistors exposed to air and encapsulated by pure PVP, PVP/PMF 50%, and PVP/PMF 100% films (all of the samples were annealed at $200\text{ }^{\circ}\text{C}$). (c) Distribution of Dirac points extracted from the I_D – V_G characteristics of 10 transistor samples for each annealing temperature.

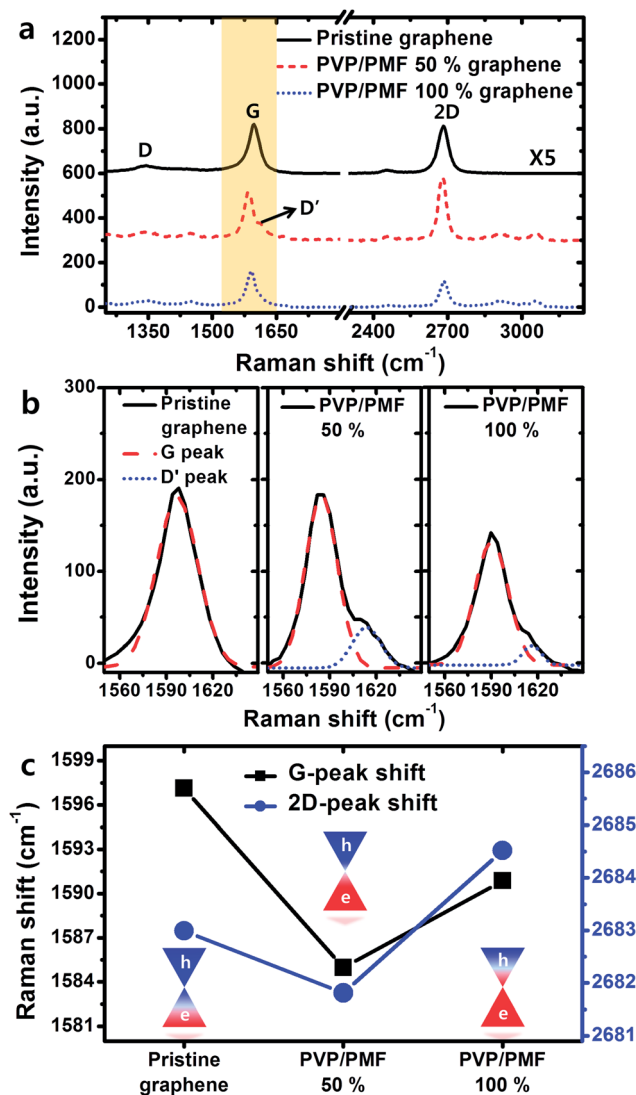


Fig. 3 (a) Raman spectra for pristine graphene on SiO_2 layer and graphene on PVP/PMF (50% and 100%) layers. (b) Lorentz fitting curves for G- and D'-peaks of the three graphene layers. (c) Raman shift of G- and 2D-peak positions in the three graphene layers.

depositing PVP/PMF 50% and 100% layers on graphene and annealing the samples, the G peaks were respectively shifted to $\sim 1584 \text{ cm}^{-1}$ and $\sim 1591 \text{ cm}^{-1}$. It is thought that the cross-linking process between graphene and PVP/PMF 50% layer seems to make the sample more intrinsic, which is also supported by Dirac point close to zero shown in Fig. 2b and c. In PVP/PMF 100% with more PMF molecules, graphene layer is expected to be n-type doped again through reaction with PMF because of its G peak up-shifted to $\sim 1591 \text{ cm}^{-1}$. This is also observable as a negative Dirac point in the Fig. 2b and c. In previous reports, the position of G peak was observed to be up-shifted in both of p- and n-type doped graphene layers.³⁷ The positions of 2D peaks in pristine and PVP/PMF 100% samples were observed at higher frequency ($\sim 2685 \text{ cm}^{-1}$), compared to that ($\sim 2680 \text{ cm}^{-1}$) in PVP/PMF 50% sample, supporting the conclusion that p-type property of pristine graphene is changed

to n-type through intrinsic as using PVP/PMF layer with higher PMF concentration. Xiaochen Dong *et al.* also reported that 2D peaks were up-shifted when p- and n-type doping was performed on graphene.³⁸

3.4 Capacitance–voltage analysis for PVP/PMF dielectric layer

Since the PVP/PMF layer needs to perform as a dielectric layer on the graphene-based devices, its dielectric properties (dielectric constant and hysteresis) are investigated through capacitance–voltage (C - V) analysis on metal-PVP/PMF-Si structure capacitors. For this experiment, PVP/PMF 50% layer was selected due to its proper chemical reaction with graphene providing Dirac point close to zero. The thickness of PVP/PMF 50% layer is 470 nm, showing quite uniform roughness with the root mean square (RMS) value of 8 nm, as shown in the scanning electron microscope (SEM) and atomic force microscope (AFM) images (Fig. 4a and b). The capacitance values were measured at 1 MHz between -15 V and 10 V , and the dielectric constants and extracted hysteresis window voltages were plotted as a function of the annealing temperature in Fig. 4c and d. Based on the C - V curves of the samples annealed at 150°C and 200°C which clearly show accumulation, depletion, and

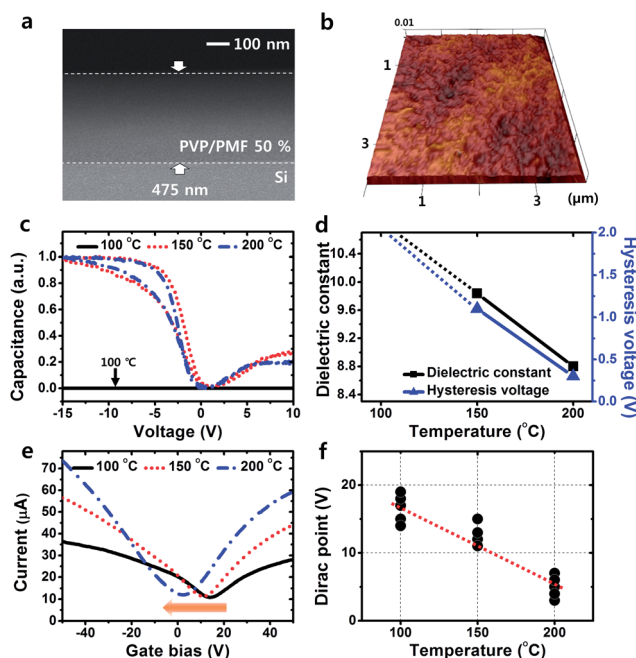


Fig. 4 Dielectric properties of PVP/PMF and carrier transporting properties of graphene devices passivated by PVP/PMF achieved at different temperatures. (a) Cross sectional SEM image of capacitor with PVP/PMF 50% layer. (b) AFM image taken on the PVP/PMF 50% layer. (c) Normalized capacitance–voltage (C - V) characteristics as a function of the annealing temperature (100°C , 150°C , and 200°C) of the capacitors with PVP/PMF 50% layer. (d) Dielectric constants and hysteresis voltages extracted from the C - V characteristics. (e) I_D - V_G characteristics of graphene transistors with PVP/PMF 50% layer, annealed at 100°C , 150°C , and 200°C . (f) Distribution of Dirac points extracted from the I_D - V_G characteristics of 10 transistor samples for each annealing temperature.

inversion regions, the PVP/PMF layer seems to work properly as a dielectric layer. However, in the sample annealed at 100 °C, dielectric behavior was not observed because of insufficient curing temperature to trigger the cross-linking process of PVP and PMF. The cross-linking process is generally known to be induced actively above 151 °C, which is the glass transition temperature of PVP.³⁹ Especially, compared to the previously reported dielectric constant (~ 4) of PVP/PMF, relatively higher dielectric constant (8–10) was observed in this 470 nm thick PVP/PMF layer because non-cured –OH groups in the PVP/PMF worked as moisture absorbers at the surface of PVP film.⁴⁰ In addition, as the annealing temperature increases, the dielectric constant and hysteresis window values are decreased. It is predicted that this is related to the –OH groups in PVP/PMF layer working as charge traps. The number of –OH groups seems to be reduced through the cross-linking process at higher curing temperature. It consequently minimizes the charge-trapping effect and decreases the hysteresis window value by achieving higher charge density on the PVP/PMF-Si interface. Besides, since the lack of –OH groups means that surface of the PVP/PMF layer is more hydrophobic, water diffusion into the higher temperature annealed PVP/PMF layer seems difficult and the probability of dielectric constant decrease through the diffused moisture is consequently expected to be high.

3.5 Electrical analysis for PVP/PMF dielectric deposited graphene transistor with different curing temperature

The effect of curing process temperature for PVP/PMF layer on graphene surface is also investigated by placing emphasis on the Dirac point of transistors fabricated on the graphene samples. PVP/PMF 50% layer was deposited on graphene transistors and the samples were annealed at 100 °C, 150 °C, and 200 °C for 30 minutes. As shown in Fig. 4e and f, the Dirac point was shifted from 16 V to 3 V with the increase of annealing temperature. It is thought that the higher annealing temperature enables more number of –OH groups in PVP/PMF to be cross-linked with those on graphene surface. As a result, PMF molecules bonded with the native –OH groups on graphene are expected to induce negative shift of Dirac point and improve hole and electron conduction. Although the curing process at 200 °C makes the PVP/PMF layer to behave as a better dielectric material and also achieve the most intrinsic graphene property, 150 °C process was selected in this work by considering the applications on flexible substrates such as PET, polyimide (PI), etc., which typically have a fairly low melting point around 150 °C to 250 °C.

3.6 Application devices: transparent, flexible and wearable graphene electronics

In order to demonstrate the advantages of PVP/PMF, graphene-based FWTEs on PET substrate were fabricated by using PVP/PMF and graphene as dielectric and channel layers (Fig. 5a) respectively. Moreover, the graphene FWTE device was successfully transferred onto a researcher's finger, as shown in Fig. 5b, showing the feasibility of the device to future wearable electronic applications. The I_D - V_G measurement was carried out

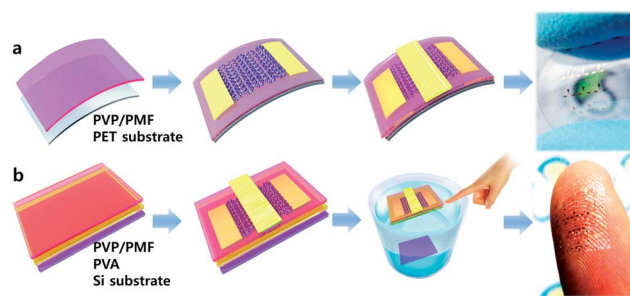


Fig. 5 Fabrication process flows for (a) flexible electronics on PET and (b) wearable electronics on a finger.

by sweeping V_G from –50 V to 100 V at $V_{DS} = 1$ V in the PVP/PMF 50% graphene FWTEs. Although the conventional V-shape I_D - V_G characteristic was obtained (dark line) as shown in Fig. 6a, its Dirac point was around 55 V indicating that graphene works as p-type material. This large positive shift of Dirac point can be explained by re-generation of –OH groups while forming the top gate stack. In order to recover the Dirac point through the cross-linking process between –OH groups of graphene and PVP/PMF layers, the devices were annealed again at 150 °C for 10 minutes and consequently the Dirac point moved back to about 1 V (blue line). In spite of the chemical reaction on graphene surface, like conventional graphene transistor devices, I_D is still linearly dependent on V_D and also modulated by V_G , as shown in Fig. 6b.

Although the top gated graphene transistor was successfully demonstrated with PVP/PMF 50% gate dielectric layer (470 nm thick), it requires high operating gate voltage and consequently makes it difficult to fabricate high performance FWTEs. Thus, we additionally scaled the thickness of PVP/PMF dielectric layer by adjusting PVP/PMF concentration in the PGMEA solution

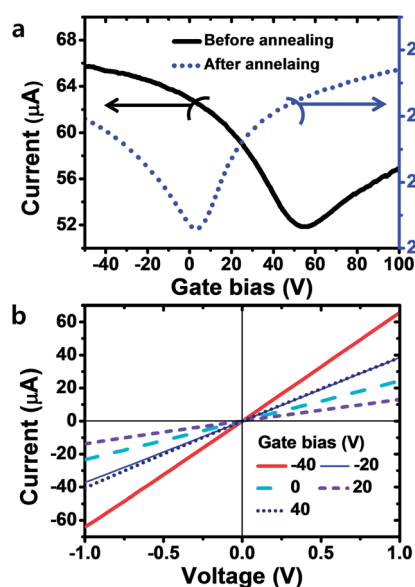


Fig. 6 Carrier transporting properties of graphene-based FWTEs. (a) I_D - V_G and (b) I_D - V_D characteristics for the graphene-based flexible transistor.

(1 wt% to 10 wt%) and investigated the transmittance/Dirac points. Fig. 7a shows SEM cross-sectional images for the scaled PVP/PMF dielectric layers (scaled from ~ 400 nm to ~ 20 nm). For estimating quantitative reduction in transmittance value owing to the additional PVP/PMF layers, ultraviolet-visible-near infrared absorption spectroscopy (UV-VIS-NIR) analysis was performed in the 300–800 nm regime and a reference graphene sample was compared with PVP/PMF 50% layer samples, as shown in Fig. 7b. The transmittance values measured at 550 nm wavelength on the (PVP/PMF) + graphene + (PVP/PMF) + PET samples are respectively 92%, 93%, 96%, 94%, and 92% for the cases of 1 wt%, 2.5 wt%, 5 wt%, 7.5 wt%, and 10 wt% PVP/PMF concentrations, indicating that the transparency of the graphene FWTEs is relatively higher than that of present FWTEs using ion gel dielectric, high-K dielectric, GO, and CNT.^{41–43} Especially, the highest transmittance value of $\sim 96\%$ was observed in the case of 5 wt% PVP/PMF concentration in PGMEA. It is thought that the scaled film thickness and the refractive index changed by dielectric constant caused the variation of transmittance values since the reduction of dielectric constants was observed as the thickness of PVP/PMF layers was scaled down.⁴⁰ Then, in order to investigate the scaling effect of PVP/PMF dielectric thickness on the electrical properties of graphene transistors with PVP/PMF gate dielectric, I_D - V_G characteristics were measured on the device samples (Fig. 8a) and the extracted Dirac points were plotted as a function of dielectric thickness in Fig. 8b. As the dielectric thickness was scaled down from 400 nm to 20 nm, Dirac point showed a decreasing tendency from 44.7 V to 0.79 V and a practical low operating gate voltage (~ 2 V) was also obtained below 120 nm thick dielectric samples. It is thought that a gate control is successfully improved through the reduction of PVP/PMF

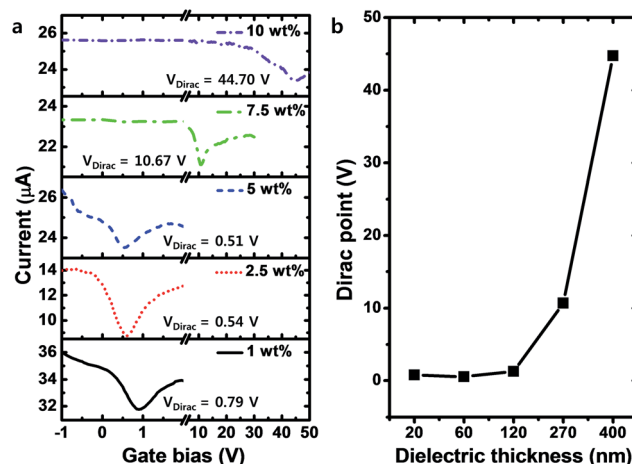


Fig. 8 Carrier transporting properties of graphene-based FWTEs according to PVP/PMF dielectric thickness. (a) I_D - V_G characteristics and (b) Dirac points as a function of the thickness of the PVP/PMF layer.

dielectric thickness, consequently demonstrating the feasibility of PVP/PMF dielectric-based graphene FWTEs.

4. Conclusion

In conclusion, PVP/PMF-based insulating layers for graphene-based FWTEs were proposed and investigated to obtain transparent and flexible gate dielectric layer and achieve an intrinsic property of graphene at sub 200 °C. The optimum conditions for fabricating graphene FWTEs using PVP/PMF insulating layer were determined as 50% PMF in PVP and 150 °C anneal through FT-IR, I - V , Raman, and C - V analyses. Finally, flexible, wearable, and transparent graphene devices were demonstrated with Dirac point close to zero using the PVP/PMF 50% layer on PET substrate and transferring it to a researcher's finger. Moreover, the PVP/PMF 50% layer was successfully scaled from 400 nm down to 20 nm by adjusting PVP/PMF concentration in PGMEA solution, consequently resulting in the reduction of operating gate voltage (~ 100 V to ~ 2 V). The transparency of graphene FWTEs showed very high values of above 92% (especially, $\sim 96\%$ in the case of 5 wt% PVP/PMF concentration in PGMEA), which are relatively higher than that of present FWTEs. Therefore, we expect that the highly transparent, scalable, and flexible PVP/PMF layers can be used for dielectric and surface passivation materials in future graphene-based FWTE devices.

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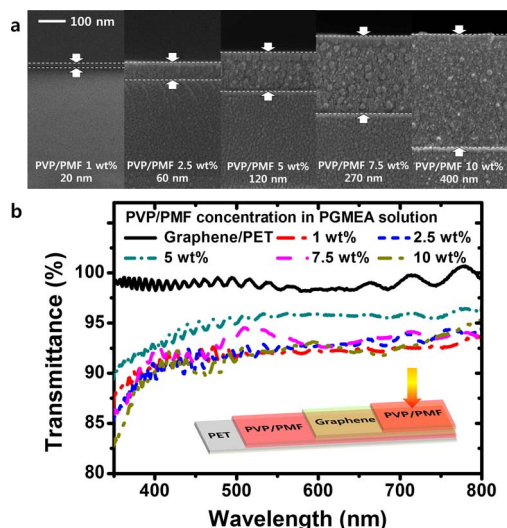


Fig. 7 Thickness and transmittance properties of the scaled PVP/PMF dielectrics. (a) SEM cross-sectional images of PVP/PMF dielectric layers respectively formed by 1 wt%, 2.5 wt%, 5 wt%, 7.5 wt%, and 10 wt% PVP/PMF solutions. (b) Transmittance spectra measured on the (PVP/PMF) + graphene + (PVP/PMF) + PET samples (Inset: structure) with different thickness of the PVP/PMF layer.

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