Capacitance-voltage and current-voltage characteristics of graphite oxide thin films patterned by ultraviolet photolithography

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Electrical characteristics of graphite oxide (GO) thin films deposited on a p-type silicon substrate were investigated to explore its potential application as a dielectric material in organic field effect transistors. Channel current in the GO films exhibited linear response with the applied bias in the positive voltage regime and increased exponentially for negative source-drain bias. This rectifying behavior arises due to the Coulombic interaction between the electrons emitted from the metal contact and the space charge region in the GO film. A clockwise hysteresis loop was observed in the capacitance-voltage characteristics due to the presence of traps at the interface. © *2009 American Institute of Physics*. [doi:10.1063/1.3280381]

Recently, thin film graphite oxide (GO) has been a subject of intense scientific investigation as it can be used as a starting material for the synthesis of graphene.[1] Extensive studies were also carried out to understand the electrical characteristics of GO thin film and to explore the possibility of integrating it with graphene based electronic circuits.[2–4] Currently existing back gated graphene based transistors (where the surface of graphene has been left uncovered) fabricated on p-type silicon substrates are not suitable for realistic device applications since a graphene transistor would require an insulator and electrode on the top of graphene. Efforts are currently underway to develop top gated graphene by fabricating contact-less top gate electrodes and alternatively by designing gates over thermally grown SiO_2 layers on graphene.[5–7] However, growing SiO_2 directly over graphene will degrade the device mobility due to interface roughness scattering and fabricating contact-less top gates may offset the advantage of cost reduction in organic field effect transistors. These shortcomings can be circumvented by coating graphene with a thin layer of dielectric material such as GO before depositing the SiO_2 layers. The identical lattice structure of GO and graphene will drastically reduce the scattering at the interfaces, and the top gated transistors can be realized without compromising the mobility of electrons in graphene. Attempts were already made to employ chemically reduced GO films as source/drain electrodes for graphene transistors instead of using the expensive and increasingly rare gold.[8] This will drastically cut down the cost of production and raises the possibility of replacing the inorganic based electronics with all carbon based electronics in future.

To realize this goal, it is necessary to explore the possibility of fabricating large scale GO pattern using UV photolithography so that it can be successfully integrated with the current silicon processing technology. One of the big challenge toward achieving this goal is to prevent the GO thin film (which is soluble in water) from degradation while subjecting it to various processing steps of photolithography. In this letter, we present the electrical characteristics of lithographically patterned GO thin films on a p-type silicon substrate by undertaking current-voltage (I-V) and capacitance-voltage (C-V) measurements.

Thin film GO was synthesized from graphite flakes by the Hummers method.[9] The thin film particles are then dried and the complete oxidation of graphite flakes was confirmed from the shift in the 002 peak in the powder x-ray diffraction measurement and also by its characteristic Raman signature.[10] For the two terminal I-V measurement, GO thin film was first dispersed in water and then drop casted over a patterned photoresist on the p-type silicon substrate (doping concentration of 10^{16} cm^{-3} coated with 500 nm of thermally evaporated SiO_2) [Fig. 1(b)]. The sample was allowed to dry in a convection oven at 75 °C for 30 min. After drying, the photoresist was removed and the thickness of the GO film was found to be 17 nm and it is measured using atomic force microscope. The length and width of the channel is 500 and 50 μm, respectively [Fig. 1(b)]. Silver contacts were then evaporated onto the patterned GO films. One such successfully patterned GO film on a silicon substrate is shown in Figs. 1(b) and 1(c). The bright regions in Fig. 1(c) are the silver contacts, which were deposited by thermal evapora-

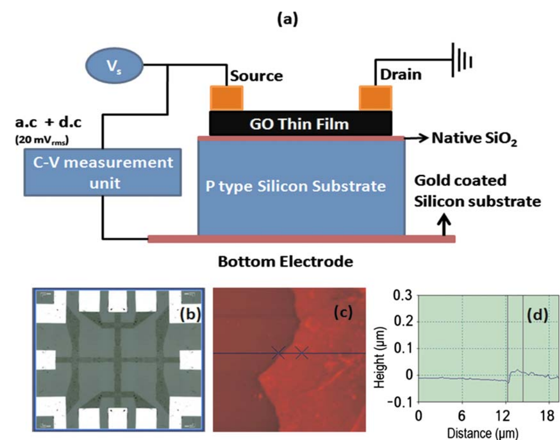

FIG. 1. (Color online) (a) Schematic diagram of the experimental setup used for undertaking two terminal I-V and C-V measurements. (b) Optical microscopic image of the GO film patterned by UV photolithography with thermally evaporated silver contacts. (c) Atomic force microscopic image of the lithographically patterned GO film and (d) its thickness profile.

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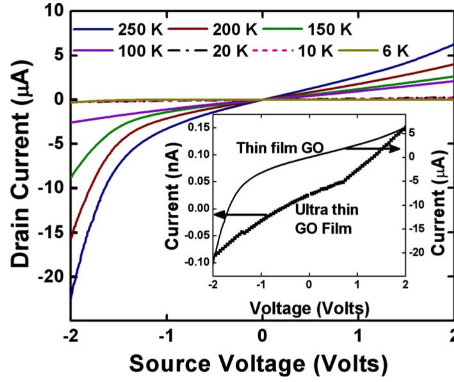

FIG. 2. (Color online) I-V characteristics of the GO thin film at different temperatures. Inset: Current-voltage characteristics of the thin film and ultrathin film GO.

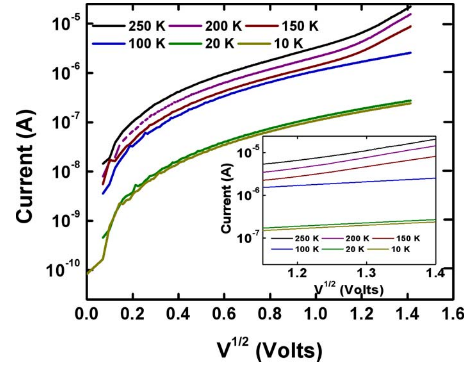

FIG. 3. (Color online) Plot of I vs $V^{1/2}$ for different temperatures. Inset: Magnified view of the plot at high electric fields.

tion. For successful patterning of GO films, the thickness of the film must be maintained below 40 nm since the films of higher thickness were found to be extremely unstable to acetone and de-ionized water rinsing.

For undertaking low temperature measurements, the thickness of the as deposited sample was increased to 0.5 μm. The films of lower thickness were found to be highly insulating below room temperature. Electrical contacts to the thin film were established using silver epoxy. The length and width of the GO channel between the contacts were 350 and 550 μm, respectively. I-V measurements at different temperatures were performed by loading the sample into a closed cycle cryostat. For the C-V measurements, 40 nm thick GO films were deposited on a bare p-type silicon wafer covered only with 1 nm of native SiO_2 layer. The capacitance measurements were taken at room temperature at a frequency of 100 kHz by connecting the sensing terminal to the silicon substrate and the signal [ac(20 mV_{rms})+dc] terminal to the silver electrode deposited on the surface of GO thin film [Fig. 1(a)]. The sweeping rate for the gate voltage was maintained at 5 mV/s for the C-V measurements.

Figure 2 shows the two terminal I-V characteristics of the GO thin film deposited on a p-type silicon substrate at different temperatures. The sample becomes highly insulating for temperatures less than 100 K and the channel current drastically reduces. As temperature is raised above 100 K, the sample undergoes a transition from insulating to semiconductor like behavior with the channel conductance increasing with increase in temperature. A linear behavior was observed in the positive voltage regime and the current increases exponentially for negative source-drain bias. The nonlinearity observed in the negative voltage regime bears the characteristic signatures of a Schottky barrier (SB).[9] It is important to note that the asymmetry in the I-V characteristics starts to show up only for temperatures greater than 100 K. Therefore the SB formed at the interface between the GO and the silver contact can be explained based on the thermionic emission model using the Richardson and Dushman equation[11]

$$J = A^*T^2 \exp\left(-\frac{q\phi_{Bn}}{k_BT}\right)\exp\left(\frac{q\Delta\phi_{\mathrm{im}}}{k_BT}\right), \quad (1)$$

where Φ_{Bn} is the SB height, A^* is the Richardson constant, $\Delta\Phi_{\mathrm{im}}$ is the barrier lowering due to image potential, T is the absolute temperature, q is the electronic charge, and k_B is the Boltzmann constant. In GO films, electrons are more likely to bind with oxygen due to its higher electronegativity and therefore an electron in GO has to surmount this attractive potential barrier before making itself available for conduction. The difference in electron affinity between carbon and oxygen atoms would create a space charge region in the GO films and the Coulombic interaction between the electrons emitted from the metal and the space charge region is likely to induce the nonlinear characteristics observed in the I-V trace. As temperature is increased, the electrons bound to oxygen can be thermally activated. In this scenario, the relationship between I and V will be governed by the equation[12]

$$I = A\exp(\beta V^{1/2})/kT, \quad (2)$$

where k is the Boltzmann constant, T is the absolute temperature in Kelvin, and β is the field lowering coefficient. The field lowering coefficient critically depends on the $\Delta\Phi_{\mathrm{im}}$ in the Richardson and Dushman equation. In the negative voltage regime, an electron leaving the silver electrode and moving into GO film experiences an attractive force (in addition to the Coulombic interaction) due to the image charges, which leads to the lowering of the SB height. On plotting log I versus $V^{1/2}$ (Fig. 3), a linear plot is obtained at high electric fields and the slope of the curve in that region is found to be greater than 2 (inset of Fig. 3) at all temperatures. Therefore the linear behavior observed in the high voltage region confirms to space charge limited conduction (SCLC) process.[13] At low and intermediate fields, the current is dominated by the charge carriers that are thermally generated and the value of the slope was found to be close to 1. In the positive voltage regime, the conduction is bulk limited and the current is dominated by the injected charge carriers giving rise to a linear I-V response.

In the inset of Fig. 2, the I-V characteristics of GO films of different thickness is shown. The thickness of the thin film is 0.5 μm and that of the ultrathin film is 17 nm. The interesting aspect of the I-V characteristics is the three orders of magnitude difference in the channel current between the thin film and ultrathin film GO. Since the channel lengths for the two films are almost similar, the result indicates that the resistance of GO films depends strongly on the thickness. The resistance variation with thickness of the film can be explained on the basis of layered structure of GO sheets. By considering a single graphene oxide layer as a simple resistor, the ultrathin GO (which is a multilayer of graphene oxide) can be regarded as an electrical equivalent of resistors in parallel.[14] Increasing the number of layers is similar to add-

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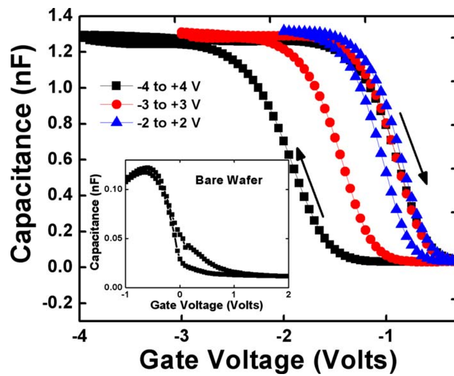

FIG. 4. (Color online) Capacitance-voltage measurement for the GO thin film at room temperature.

ing an additional resistor, which in turn increases the net current flowing across the channel. Therefore the difference in the number of individual graphene oxide layers between thin film (thickness 0.5 μm) and ultrathin film (thickness 17 nm) samples could be the plausible reason for the channel conductance to differ by three orders of magnitude.

To ascertain the nature of interface states formed at the GO/SiO_2 junction, C-V measurements were carried out in room temperature and the results are shown in Fig. 4. In the C-V measurement, the measurement error was estimated to be approximately less than 2% at a gate bias of ± 4 V by taking into account the effects of gate tunneling current and channel resistance. A clockwise hysteresis loop was observed on cyclically sweeping the gate bias. The measurement was then repeated by increasing the maximum gate voltage (V_{gmax}) to which the sweep was returned. On incrementing the range of V_{gmax} from 2 to 4 V, the area of the hysteresis loop increased proportionally. The bare wafer did not show any such hysteresis behavior. The hysteresis opening in the C-V trace is a clear indication that there are considerable amount of charged traps (Q) are present in GO films. The amount of charges that gets accumulated in the traps as V_{gmax} was increased can be determined by using the equation $Q = C \times \Delta V_{FB}/A$, where ΔV_{FB} is the flat band voltage shift and A is the area of gate contact. The trapped charge density for $V_{gmax}=4,3$, and 2 V was found to be 6.62×10^{11}, 3.52×10^{11}, and 7.9×10^{10} charged traps/cm^2, respectively. The high density of charged traps is expected for chemically synthesized GO thin films as many structural defects will be developed during the oxidation process. These defects may be vacancy or an interstitial defect. These defect centers act as Coulombic scattering centers when charged and will be oriented in random direction. The Coulombic potentials from these charged traps will increase proportionally with increase in V_{gmax} as more and more electrons injected from the gate electrode are trapped in the defect centers. The potential from the traps partially screens the gate voltage and therefore induces a negative shift in V_{FB}.

From our study, it is clear that a large number of charged trapping centers and space charge regions that are present in the GO film significantly affect its electrical characteristics. This will give rise to undesirable effects when graphene oxide films are to be used as a dielectric material for graphene. Recently a method has been proposed to repair the structural defects in graphene oxide films.[15] With this breakthrough, the goal of realizing all carbon based transistors is very much closer to reality.

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