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Exploring Electrostatic Confinement Transport in MoS_2/WSe_2 Heterostructure via Triple-Gated Point Contact Device

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The exponential development in quantum phenomena is directly correlated with the decreasing size of nano-semiconductor transistors. Consequently, the use of a quantum structure that deviates from traditional transistor types becomes imperative. Electrostatically defined nanoscale devices within 2D semiconductor heterostructures serve as foundational elements for diverse quantum electrical circuits. Van der Waals heterostructures, distinguished by atomically flat interfaces and inherent 2D characteristics, offer advantages such as large-scale uniformity, flexibility, and portability over conventional bulk semiconductor heterostructures. Herein, the intricate electronic behavior of a MoS_2/WSe_2 encapsulated heterostructure governed by split-gate and middle-gate configurations is investigated, revealing a distinctive step-like current profile at a low temperature of 77 K. The observed four regimes in the current highlight the impact of quantum confinement induced by reduced lateral dimensions, coupled with precise electrostatic confinement controlled by gate voltages. The temperature dependence of the phenomena emphasizes the role of thermal effects on carrier scattering mechanisms. In addition, the pinch-off characteristics with different temperatures, middle-gate voltages, and drain biases are explored. This study contributes to a deeper understanding of electrostatic effects in 2D transition metal dichalcogenide heterostructures and holds promise for the development of advanced electronic devices with tailored confinement for enhanced functionalities.

1. Introduction

Transition metal dichalcogenides (TMDs) based 2D materials have demonstrated significant progress in the field of nanoelectronics, attributed to their mechanical, optical, and electronic properties.[1–4] Owing to their flexibility and atomically thin nature, these materials can be artificially combined into heterostructures, offering unique opportunities to control charge carriers at the nanoscale, influencing phenomena such as optical excitons, superconductivity, and magnetism.[5–8] In the research of quantum charge transport, narrow contraction, and depletion in two electrically conduction areas have been realized by quantum point contact (QPC) using split-gate geometry.[9–14] Among the various TMD heterostructure devices designed, the split-gate stands as one of the simplest and remarkably effective solutions to control the quantum flow of electrons in a confined region. Its core function lies in the transformation of 2D electron transport into a 1D regime through the

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creation of a quantum point contact.[15,16] However, complementing this, the need for the middle gate is crucial to play a significant role in controlling the confined 1D current within the heterojunction region. An essential element in comprehending and using the electrical characteristics of heterostructures based on TMDs is exploring the transport of electrostatically confined charges in devices with split-gated point contacts along with controlling the charge carriers by middle-gate. Triple-gated devices use the middle-gate voltages to manipulate the electrostatic potential, hence facilitating accurate control of the confinement and transportation of charge carriers inside a narrow channel.[17,18] A further captivating phenomenon that arises because of electrostatic confinement is the detection of discrete increments in the flow of electric charge. This control leads to the emergence of distinct energy levels, which are seen as step-like patterns in the current.[19,20] The quantized steps mentioned in the statement provide valuable insights into the energy spectrum and transport characteristics of restricted states. Electrostatically split-gate-defined QPC-based graphene/hBN structures have been demonstrated.[21] However, in contrast to graphene, molybdenum disulfide (MoS_2) and tungsten diselenide (WSe_2) have attracted considerable interest due to their controllable band gap and superior electrostatic tunability. Many quantum phenomena such as exciton condensation, quantum dots, and band-to-band tunneling are primarily due to the emergence of synergistic effects of these materials resulting in improved functionalities.[22–26]

In this study, we demonstrate an examination of a triple-gated point contact device that relies on a heterostructure composed of MoS_2 and WSe_2. The primary objective is to explore the electrostatic confinement transport shown by this distinctive configuration. The electron flow in the device is controlled and confined by varying the voltage on the triple-gate in a temperature regime between 77 and 300 K. By manipulating the split-gate voltage, the step-like feature in current is observed. The middle gate is used for tuning the carrier concentration in the MoS_2/WSe_2 heterostructure. We also study the dependence of the point-contact formation on the middle-gate voltage. In addition, the pinch-off characteristics are investigated with different temperatures, middle-gate, and drain biases for further understanding of the electrostatic transport in the device. These findings provide valuable insights into the fundamental mechanisms that govern the transportation of charges in this heterostructure.

2. Results and Discussion

Figure 1a illustrates our fabrication process initiating with electron beam lithography and titanium (Ti)/gold (Au) metallization to define the split-gate, which forms the point-contact, and the middle-gate utilized to control carrier concentration in the heterostructure region on a 285 nm SiO_2/Si substrate. The scanning electron microscope (SEM) image reveals a gap of ≈100 nm in the triple-gate structure. To serve as a dielectric material, we employ a mechanically exfoliated thick hBN flake, transferred onto the triple-gate using the polydimethylpolysiloxane (PDMS) dry transfer method. Subsequently, we use the PDMS dry transfer technique to carefully place a thin flake of MoS_2 on top of the hBN flake, followed by a WSe_2 flake to define the MoS_2/WSe_2 heterostructure, with an additional top hBN layer for encapsulation (Figure 1b). The edge contact technique, coupled with electron-beam lithography and indium (In)/Au metallization, is employed to define the drain and source contacts on each layer and heterostructure region (Figure 1c). Finally, the device is equipped with In low-work-function electrodes, serving as drain and source contacts (Figure 1d).

In Figure 1e, we present the energy band diagrams of the MoS_2/WSe_2 heterostructure, classified as type II. This classification signifies a distinctive energetic arrangement where the conduction band minimum of one constituent material (MoS_2) aligns with the valence band maximum of the other material (WSe_2). Consequently, this alignment triggers electron and hole transfer phenomena across the heterointerface, with the primary goal being the equilibration of Fermi levels. This equilibration process leads to the formation of a depletion region, indicating reduced charge carrier concentrations within both material layers. Ideally, MoS_2 would exhibit n-type conductivity, reflecting an excess of electrons, while WSe_2 would exhibit p-type conductivity, reflecting an excess of holes.

Raman spectra of MoS_2, WSe_2, and the MoS_2/WSe_2 heterostructure are acquired in an ambient environment, employing laser excitation with a wavelength of 532 nm (Figure 1f). The Raman spectrum of MoS_2 features two peaks: the E^1_{2g} peak located at ≈387 cm^{-1}, corresponding to the in-plane vibrational mode of both metal and chalcogen atoms, and the A_{1g} peak at ≈412 cm^{-1}, representing the out-of-plane vibrational mode of chalcogen atoms.[27] In the WSe_2 Raman spectrum, the presence of two primary vibrational modes, the E^1_{2g} peak located at ≈253 cm^{-1} and the A_{1g} peak at ≈262 cm^{-1}, indicates that the WSe_2 flake comprises few layers.[28] The Raman spectrum of the overlapped region includes both MoS_2 and WSe_2 peaks. To confirm the layer thickness of the MoS_2 and WSe_2 flakes, atomic force microscopy (AFM) was conducted, revealing thicknesses of 5.4 and 3.3 nm, respectively (Figure S1, Supporting Information).

Initially, the electrostatic effect of the point contacts in our device was examined as demonstrated in **Figure 2**. Throughout all measurements discussed in this manuscript, a consistent potential was maintained for both electrodes defining the split gate. In Figure 2a, the step-like current is observed with four distinguishable regimes while sweeping split-gate voltage (V_{SG}) with a fixed drain voltage (V_D) of 1 V at 77, 100, and 150 K. As the V_{SG} is decreased, the depletion of electrons beneath the gate-electrodes occurs, leading to a reduction in the current and the formation of a narrow constriction, referred to as the point contact. The electrostatic confinement of electrons within the formed point-contact manifests as a parabolic feature in the confinement potential. To clarify the change of the electrical transport under electrostatic modulation, the transconductance (g_m) is extracted by taking the derivative of the drain-to-source current (I_D) with respect to the V_{SG} (dI_D/dV_{SG}) and then plotted as a function of V_{SG} (Figure 2b). The g_m characteristics of our device present three distinct peaks corresponding to the three steps in the on-state of the device. This behavior is notably distinct from that of standard field-effect transistors (FETs), suggesting a unique interplay of quantum and electrostatic effects in our device. This peculiar behavior is a consequence of the reduction in V_{SG}, effectively lowering the available states in the constriction through the Fermi level. This reduction in available states leads to a gradual decrease in the current, explaining the observed step-like feature in the

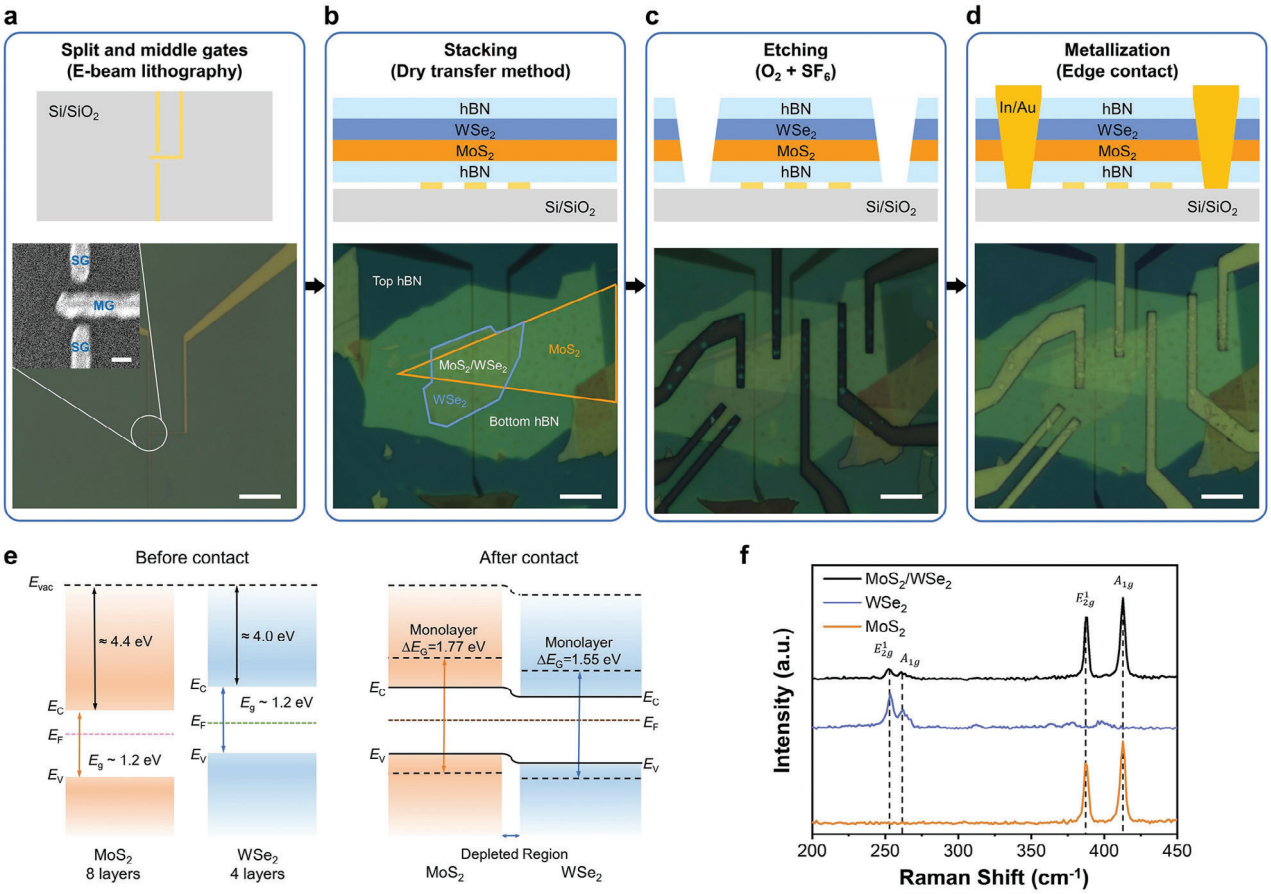

Figure 1. Fabrication process and characterization of hBN/MoS_2/WSe_2/hBN encapsulated heterostructures with triple-gated quantum point contact device. a) Electron-beam lithography was employed to define ≈10-nm thick split and middle gates on a Si/SiO_2 substrate. The scale bar is 5 µm. The inset presents the SEM image revealing the gap of the triple-gate. (Inset scale bar, 200 nm). b) Layer-by-layer assembly of hBN/MoS_2/WSe_2/hBN on the triple-gate structure. c) Plasma etching for edge contacts of the MoS_2/WSe_2 heterostructure. d) Metallization is achieved using In/Au layers (10/30 nm) to establish edge contacts for electrical characterization in heterostructure regions and individual layers. e) Energy band diagrams of MoS_2 (8 layers) and WSe_2 (4 layers) before and after contact, illustrating the formation of depletion. f) Raman spectra of MoS_2, WSe_2, and MoS_2/WSe_2 heterostructure.

on-state.[15,29] Figure 2c offers a deeper insight into the electrostatic confinement in the MoS_2/WSe_2 heterostructure under various split-gate biases. When V_{SG} falls below −10 V, both the MoS_2 and WSe_2 channels in the n-type heterojunction are entirely closed due to the substantial bias applied to the V_{SG}. This illustrates our effective control over the electronic states in both materials (i). At $V_{SG} = -5$ V, the 1D channel opens up, which facilitates the confinement of electrons and enables the flow of step-like current. This bias voltage provides ideal conditions for observing step-like features in electron transport (ii). However, at $V_{SG} = 5$ V, the step-like current becomes nearly imperceptible. This outcome results from the widening of the channel, which diminishes the confinement of electrons (iii). Finally, when V_{SG} exceeds 10 V, the current no longer exhibits step-like phenomena and instead reaches a saturation point (iv). This transition indicates a fundamental change in the underlying electronic structure and transport properties of the device under these extreme bias conditions. These comprehensive observations and analyses contribute to a deeper comprehension of the intricate interplay between quantum and electrostatic effects in our device, paving the way for advanced applications in nanoelectronics.

To understand the pinch-off characteristics of the MoS_2/WSe_2 heterostructure manipulated by the triple-gate configuration, our measurements were conducted at 77 K while systematically varying the V_{SG} with the fixed middle-gate voltage (V_{MG}). These experimental conditions provide crucial insights into the behavior of charge carriers within this heterostructure. At 77 K, our device exhibited intriguing step-like current behavior as the V_{SG} was swept from −20 to 20 V, as illustrated in **Figure 3a**. This distinct feature unequivocally confirms the discrete nature of charge carriers confined within the narrow channel.[19,29,30] This step-like feature arises from discrete energy levels within the channel region due to the strong confinement of charge carriers within the 2D material heterostructure. This discrete behavior of charge carriers is a pivotal factor contributing to the observed phenomena. Conversely, at 300 K, the device displayed n-type behavior, indicating an abundance of free electrons. As we applied increasingly positive V_{MG} values, we observed a reduction in the on/off ratio of the device. This effect can be attributed to the accumulation of charge carriers within the channel region. Elevated V_{MG} values lead to an increase in the number of free electrons within the device. This accumulation results in a decreased on/off

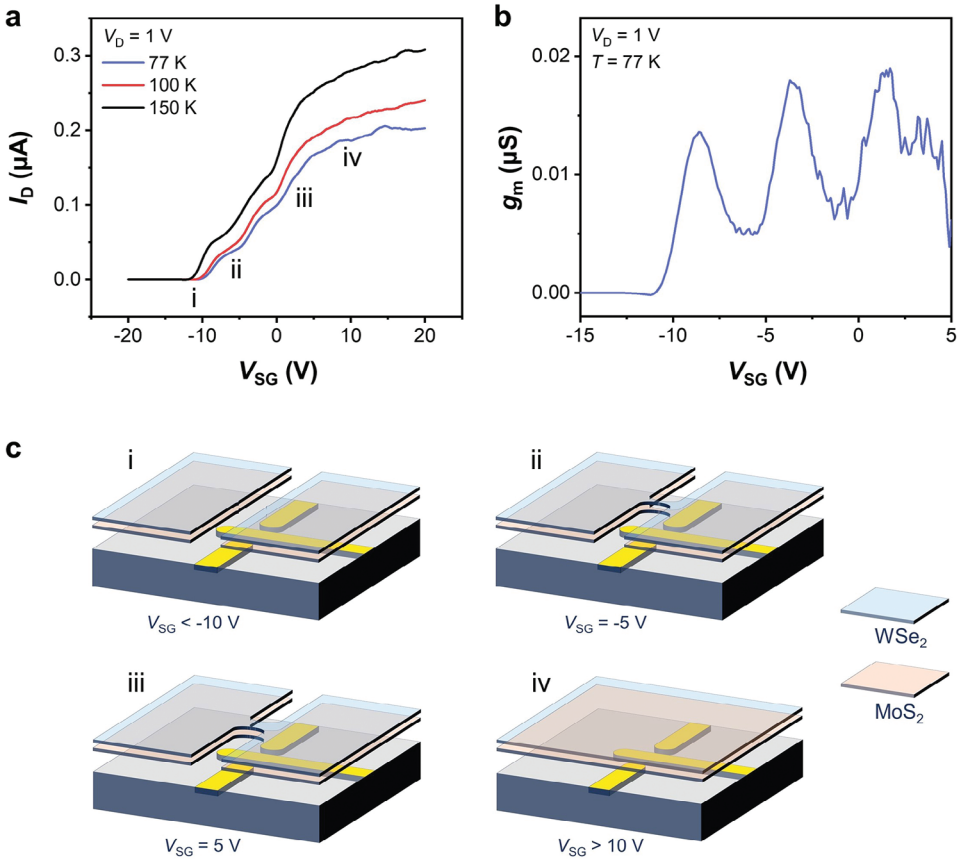

Figure 2. Electrostatic confinement is controlled by the triple-gated structure. a) I_D–V_{SG} curve for the triple-gated device as a function of V_{SG} with V_D = 1 V at 77, 100, and 150 K. b) Transconductance versus V_{SG} at 77 K exhibiting three peaks corresponding to the three steps in the I_D–V_{SG} curve. c) Schematic diagrams demonstrating the electron-depleted state of the MoS_2 and WSe_2 layers according to the four regimes shown in the I_D–V_{SG} curve without considering the middle gate. (i) In the case of $V_{SG} < -10$ V, electrons in the MoS_2 and WSe_2 layers are all depleted, and electrons no longer flow between the source and drain. (ii) When $V_{SG} = -5$ V, a 1D current path is formed, and current flows. (iii) In the case of $V_{SG} = 5$ V, the passage of current expands, and more electrons move. (iv) In the case of $V_{SG} > 10$ V, the 1D channel is changed to 2D, and saturation is performed.

ratio, leading to a less distinct differentiation between the on and off states of the device, as depicted in Figure S2 (Supporting Information). To gain a more comprehensive understanding of the pinch-off characteristics in our device under triple-gate control, the transconductance plot presented in Figure 3b shows the oscillations as a function of both V_{SG} and V_{MG} at 77 K. The presence of well-defined steps for all V_{MG} affirms the persistence of the electrostatic confinement at lower temperatures. Figure 3c demonstrates schematic diagrams at $V_{MG} = -10$ and 10 V to give a better explanation of the effect of the middle-gate modulation. When $V_{MG} = -10$ V is applied, the extent of the constriction region in the triple-gated MoS_2/WSe_2 structure diminishes. In the realm of field-effect devices, the carrier density is proportional to V_{MG}. Lower V_{MG} results in a narrower channel and the constriction having fewer available states for transport compared to higher V_{MG}. In addition, electrons of both MoS_2 and WSe_2 are depleted, which results in a narrower channel compared to the channel applied $V_{MG} = 10$ V. This phenomenon leads to a proportional reduction in the span of V_{MG} necessary to deplete the states, causing the depletion of electrons in the constriction and the initiation of the tunneling regime at higher V_{SG}. To confirm the electrostatic confinement of the MoS_2/WSe_2 heterostructure under the triple-gate control, we fabricated a sample with surface contacts, and the step-like current with four different regimes is also observed (Figure S3, Supporting Information). The similar electrical characteristics of both devices with edge and surface contacts affirm that the electrostatic confinement effect by using this triple-gate configuration is consistent and reproducible. This confinement at lower temperatures signifies the captivating quantum transport behavior of confined charge carriers within the MoS_2/WSe_2 heterostructure.

To further understand the pinch-off characteristics of the MoS_2/WSe_2 heterostructure controlled by the triple-gate, as shown in **Figure 4**, we plotted the temperature dependence of pinch-off voltage (V_{po}) referring to the V_{SG} at which the channel is nearly closed, restricting the flow of electrons through the constriction. V_{po} in a semiconductor device decreases with an increase in temperature due to the temperature dependence of carrier mobility. As illustrated in Figure 4a, V_{po} increases with increasing V_{MG}. When a positive V_{MG} is applied, it introduces additional positive charge carriers (holes) into the channel, primarily in the WSe_2 region. This positive V_{MG} tends to counteract the electron accumulation in the MoS_2 region. The overall effect on V_{po} depends on the relative influence of the positive middle

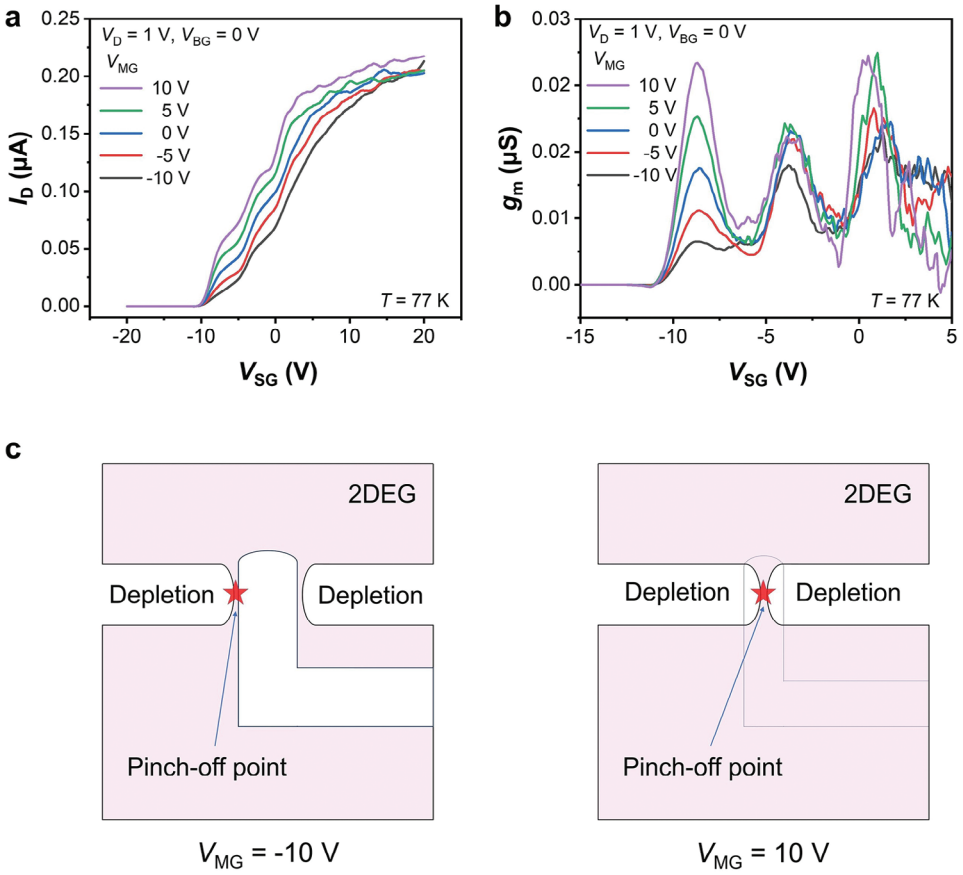

Figure 3. Pinch-off characteristics of the triple-gated MoS_2/WSe_2 device. a) I_D–V_{SG} curves for the triple-gated device as a function of V_{SG} at V_D = 1 V controlled by the middle-gate ranging from −10 to 10 V at 77 K. b) A surface plot of the step-like currents at 77 K for a series of V_{SG} and V_{MG}. c) Schematic diagram illustrating the effect of the middle gate on the pinch-off characteristics. At V_{MG} = −10 V, the constriction region diminishes, leading to a narrower channel due to the depletion of electrons in both MoS_2 and WSe_2. In contrast, at V_{MG} = 10 V, the channel exhibits a wider configuration with increased available states for transport.

gate on the holes in WSe_2 compared to its influence on the electrons in MoS_2. Since WSe_2 is ambipolar with n-type carriers more dominant (Figure S4a, Supporting Information), applying a positive V_{MG} is likely to increase the V_{po}. As depicted in Figure 4b, it is observed that V_{po} increases with a reduction in V_D, characteristic of the transport behavior across a barrier. This behavior is characterized by a proportional relationship between the current flowing through the barrier, the voltage across the barrier, and the transmission coefficient of the barrier.[15] Consequently, with an increase in V_D, it is necessary to reduce V_{SG} to disrupt

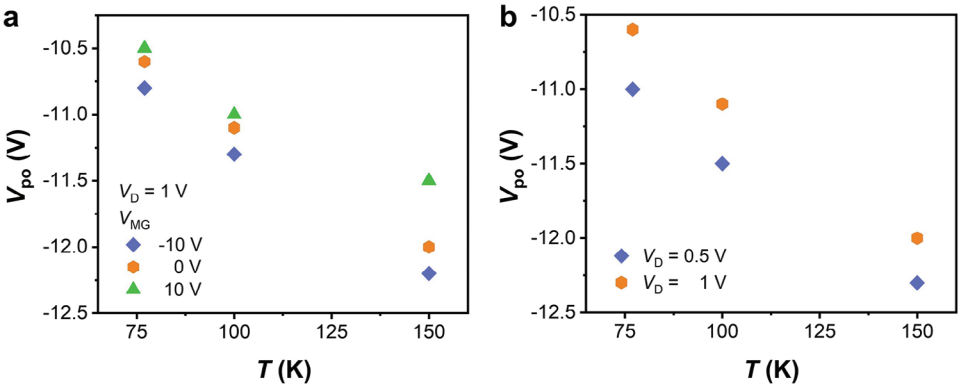

Figure 4. Temperature dependence of the pinch-off voltage at different middle-gate voltages (a) and drain biases (b) of the triple-gated MoS_2/WSe_2 heterostructure.

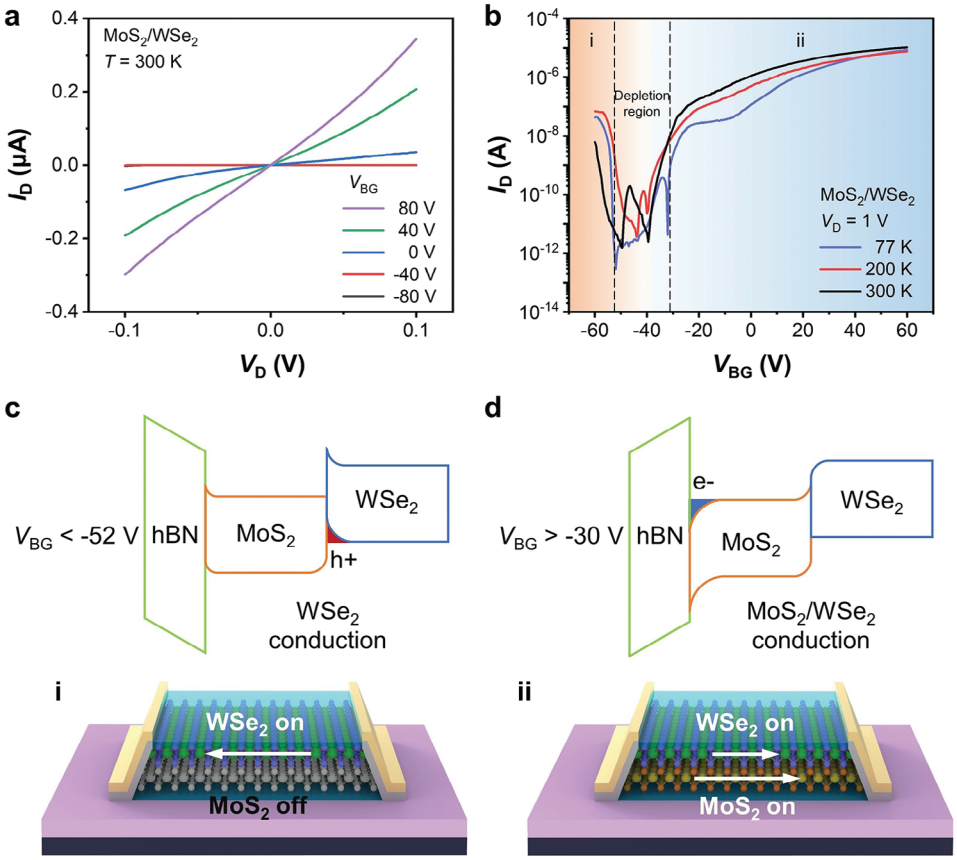

Figure 5. Electrical transport properties of the MoS_2/WSe_2 heterostructures with V_{BG} control. a) I_D–V_D characteristics of the MoS_2/WSe_2 heterostructures with edge contacts depending on the different V_{BG} ranging between −80 and 80 V in 40 V steps at 300 K. b) I_D–V_{BG} characteristics of the MoS_2/WSe_2 heterostructures for V_{BG} ranging from −60 to 60 V at 77, 200, and 300 K with a drain voltage of 1 V. c,d) Schematic band diagram and device schematic showing the band structure and current flow in WSe_2 hole carriers at $V_{BG} < -52$ V (c) and MoS_2/WSe_2 heterostructure electron carriers at $V_{BG} > 30$ V (d).

the transmission of charge carriers, accomplished by elevating the potential barrier within the device.[15]

In **Figure 5**, we delve into a thorough investigation of the charge transport behavior within MoS_2/WSe_2 heterostructures under the influence of V_{BG} control. The presented I–V output characteristics, as shown in Figure 5a, illustrate the quasi-ohmic behavior observed within the MoS_2/WSe_2 channels when subjected to varying applied voltages at a temperature of 300 K. To ascertain the polarity of these heterostructures, we conducted separate measurements on the single-channel FETs for both MoS_2 and WSe_2, as depicted in Figure S4 (Supporting Information). Notably, MoS_2 exhibits an n-type polarity when subjected to edge contact, as detailed in previous studies.[31] Conversely, WSe_2, despite utilizing a low work function metal like In, displays ambipolar behavior. This behavior is indicative of Fermi-level pinning at the edge-contacted WSe_2.[32,33] Consequently, the transfer curves of the MoS_2/WSe_2 heterostructures reveal ambipolar behavior at three distinct temperatures: 77, 200, and 300 K (Figure 5b). This intriguing phenomenon is attributed to the transport of electrons through the MoS_2 channel and holes through the WSe_2 channel.

For a more comprehensive understanding of this ambipolar transport, we refer to Figure 5c,d. In the positive gate regime, a positive gate electric field induces downward band bending, leading to electron accumulation within MoS_2 and simultaneous charge carrier depletion in WSe_2 (Figure 5c). This results in a significant exponential increase in current flow through the MoS_2 channel, as is evident in the transfer characteristics. Conversely, during the negative gate regime, reverse band bending is observed due to the negative gate electric field. This induces hole accumulation within WSe_2 and subsequently forms a current channel (Figure 5d). Furthermore, it's worth highlighting a distinctive characteristic of our MoS_2/WSe_2 heterostructure,[34,35] which is its reasonably wide off-state window of ≈20 V, as seen in Figure 5b. Additionally, the on/off ratio reaches $\approx 10^4$ and 10^6 for negative and positive V_{BG}, respectively. This unique feature holds significant promise for applications in logic circuits.[36–38]

3. Conclusion

In summary, we have reported the electrical transport of the MoS_2/WSe_2 encapsulated heterostructure, electrostatically manipulated by split-gate and middle-gate configurations. Our methodology leverages a split gate configuration to exert comprehensive control over electron transport, effectively transitioning it from a 2D regime to a 1D regime. This transition is achieved by applying a negative bias to each of the 1D channels, allowing for

the modulation of the n-type channel width, and subsequently employing a positive bias to regulate the p-type channel width. The middle gate serves a critical role in independently opening or closing the 1D channel, irrespective of the split gate's state. Consequently, this unique combination of split and middle gates affords us the capability to induce a distinct step-like current profile at a temperature of 77 K. The identified four regimes in the current underscore the significant interplay of quantum confinement, attributed to reduced lateral dimensions, and precise electrostatic confinement controlled by gate voltages. These findings underscore the immense potential of atomically thin heterojunctions in paving the way for innovative quantum device applications. In particular, our approach opens up exciting possibilities for the realization of quantum transistors based on TMD materials, with promising prospects in the realms of spintronics, valleytronic devices, and the development of valley spin qubits. This work represents a significant step forward in harnessing the quantum properties of TMD materials for advanced electronic applications and lays the foundation for further exploration in this cutting-edge field.

4. Experimental Section

Growing MoS_2 Crystal Using the Flux Method: The flux method was used to grow high-purity MoS_2 crystals, utilizing tin (Sn) as the flux material. This flux material, characterized by its low melting point, aids in dissolving solute substances for the ensuing chemical reaction. Subsequently, the flux material was eliminated from the crystals by subjecting the hot ampoule to centrifugation immediately after removal from the furnace, without allowing it to cool down.

The source materials, namely Mo (Sigma-Aldrich purity 99.99%), S (Sigma-Aldrich purity 99.99%), and Sn (Sigma-Aldrich purity 99.99%), were mingled in specific proportions in an alumina crucible. Following this, the crucible was placed inside a quartz ampoule in an argon (Ar) environment, all inside a glovebox. To absorb any excess solvent during centrifugation, a cylinder made of high-purity (99.99%) SiO_2 quartz wool with exceptional insulating properties was placed 1 cm above the alumina crucible.

After evacuation and sealing, the ampoule was subjected to a high-temperature furnace set at 1150 °C, with a heating rate of 50 °C per hour. It remained at this temperature for 36 h. Subsequently, a cooling rate of 2.5 °C per hour was employed to reach a temperature of 1000 °C. The resulting ampoule was then subjected to centrifugation, and the grown crystals were utilized in the fabrication of devices.

Growing WSe_2 Crystals Using the Flux Method: The flux method was utilized for the growth of high-purity WSe_2 crystals, with selenium (Se) serving as the self-flux material.[39] This flux material, with its low melting point, facilitated the dissolution of solute for the chemical reaction and could be conveniently removed from the crystals through immediate centrifugation of the hot ampoule upon removal from the furnace, without allowing it to cool.

The source materials, W and Se (Alfa Aesar purity 99.999%), were accurately measured and mixed within an alumina crucible. This crucible was then placed inside a quartz ampule within an Ar environment, all inside a glovebox. To absorb any excess solvent during centrifugation, a cylinder made of high-purity (99.99%) SiO_2 quartz wool, known for its excellent insulating properties, was placed 1 cm above the alumina crucible.

After vacuuming and sealing, the ampoule was inserted into a high-temperature furnace set at 1100 °C, with a heating rate of 50 °C per hour. It remained at this temperature for 48 h. Subsequently, the ampoule was gradually cooled to 450 °C at a rate of 2.5 °C per hour. The resulting ampoule was then centrifuged at 2000 rpm for 60 s. Finally, the crystals were analyzed using Raman spectroscopy to measure their formation and quality.

Fabrication of Mechanically Exfoliated Devices: MoS_2 and WSe_2 are used as channel materials that are grown by the self-flux method in the lab, whereas hBN was obtained from bulk crystals grown at the National Institute of Materials Science and Technology in Japan. Using the photolithography method, a highly p-doped 285 nm Si/SiO_2 substrate was used to draw an outer electrode pattern, and Au/In metal layers were deposited using an electron beam evaporator before being lifted off in acetone. An electron beam lithography was performed to draw split and middle-gates of ≈10 nm thickness in ratios of Ti/Au (2/8 nm) and deposited using an electron-beam evaporator (Korea Vacuum Tech. KVT-2004) defining the point-contact and middle-gate to control the carrier concentration in the heterostructure region on 285 nm Si/SiO_2 substrate. A mechanically exfoliated thick h-BN flake was transferred as a dielectric material on top of the triple-gate by the PDMS dry transfer method. Later, with the PDMS dry transfer technique, a thin flake of MoS_2 was carefully placed on top of the hBN flake, followed by the WSe_2 flake to define the MoS_2/WSe_2 heterostructure. Finally, a top hBN was transferred to encapsulate the flakes. The sample was then cleaned in chloroform, followed by acetone and isopropyl alcohol, and dried up using a nitrogen gun. For the edge-contacted device, the edge-contact technique was used to define the drain and source contacts on each layer and heterostructure region using electron-beam lithography, followed by the In/Au (10/30 nm) metallization. For the surface-contacted device, the surface contacts (In/Au 10/30 nm) were designed by electron-beam lithography as the source and drain on each material.

Characterization of Devices: After device fabrication, the thicknesses of the MoS_2 and WSe_2 were analyzed by AFM in noncontact mode. The Raman spectra were obtained using a micro-Raman spectrometer with a 532 nm laser under ambient conditions to characterize the flakes. Current–voltage (*I–V*) measurements of all the electrical devices were performed with a Keithley 4200-SCS parameter analyzer under vacuum conditions below 20 mTorr system at room temperature (≈300 K) and low-temperature (≈77 K) to determine the contact and channel charge polarity. The V_{BG} of all the devices in our study was applied through an hBN (≈35 nm)/SiO_2 (285 nm) (C_{ox} = 1.21 × 10^{-8} F cm^{-2}) dielectric stack. To measure the heterostructure through the middle and split-gates, the split-gate is swept while changing the drain bias and middle-gate voltage stepwise to control the carrier concentration in the channel over different temperatures ranging from 77 to 300 K.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

Research data are not shared.

Keywords

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