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Tunable Electron and Hole Injection Enabled by Atomically Thin Tunneling Layer for Improved Contact Resistance and Dual Channel Transport in MoS_2/WSe_2 van der Waals Heterostructure

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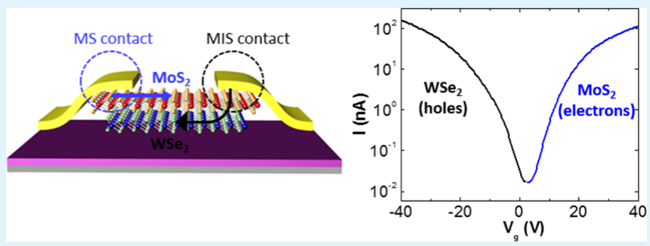
Supporting Information

ABSTRACT: Two-dimensional (2D) material-based heterostructures provide a unique platform where interactions between stacked 2D layers can enhance the electrical and opto-electrical properties as well as give rise to interesting new phenomena. Here, the operation of a van der Waals heterostructure device comprising of vertically stacked bilayer MoS_2 and few layered WSe_2 has been demonstrated in which an atomically thin MoS_2 layer has been employed as a tunneling layer to the underlying WSe_2 layer. In this way, simultaneous contacts to both MoS_2 and WSe_2 2D layers have been established by forming a direct metal−semiconductor to MoS_2 and a tunneling-based metal−insulator−semiconductor contacts to WSe_2, respectively. The use of MoS_2 as a dielectric tunneling layer results in an improved contact resistance (80 kΩ μm) for WSe_2 contact, which is attributed to reduction in the effective Schottky barrier height and is also confirmed from the temperature-dependent measurement. Furthermore, this unique contact engineering and type-II band alignment between MoS_2 and WSe_2 enables a selective and independent carrier transport across the respective layers. This contact engineered dual channel heterostructure exhibits an excellent gate control and both channel current and carrier types can be modulated by the vertical electric field of the gate electrode, which is also reflected in the on/off ratio of 10^4 for both electron (MoS_2) and hole (WSe_2) channels. Moreover, the charge transfer at the heterointerface is studied quantitatively from the shift in the threshold voltage of the pristine MoS_2 and the heterostructure device, which agrees with the carrier recombination-induced optical quenching as observed in the Raman spectra of the pristine and heterostructure layers. This observation of dual channel ambipolar transport enabled by the hybrid tunneling contacts and strong interlayer coupling can be utilized for high-performance opto-electrical devices and applications.



KEYWORDS: *heterostructure, dual channel, MoS_2, WSe_2, tunneling*

1. INTRODUCTION

Two-dimensional (2D) materials have emerged as promising candidates for future nanoelectronic applications as well as interesting research topic for fundamental science and applied physics.[1,2] The 2D material family constitutes of a full variety of material types, ranging from insulators[3,4] and semiconductors[5,6] to semimetals[7] and superconductors.[8] These materials possess a strong in-plane covalent bond which provides in-plane stability, whereas the weak out-of-plane van der Waals force allows isolation of a 2D monolayer. These isolated monolayers can be conveniently stacked to form several configurations of heterostructures based on different 2D materials.[9,10] Heterostructures based on 2D materials have been studied to explore new physics such as super-lattice Dirac points[11] and Hofstadter butterfly patterns[12,13] as well as new device configurations like tunneling transistors,[14] ambipolar transistors,[15] and ultrathin photodetectors.[16] One of the major challenge in realizing these innovative devices based on 2D materials for practical applications is high contact resistance offered by 2D materials.[17,18] MoS_2 and WSe_2 are two prominent members of the 2D material family and a great deal of experimental work has been conducted to improve the contact resistance in these 2D materials. This includes the use of optimum work function metal,[19] the use of graphene electrodes,[20] phase-engineered contacts,[21] degenerate doping of the contact area,[22−24] ionic-gate doping of the contact area,[25] and plasma-assisted functionalization.[26] Recently, a new kind of 2D heterostructure has been proposed[27,28] and studied to achieve low contact resistance in MoS_2,[29,30] where an ultrathin dielectric layer (h-BN) has been inserted as a

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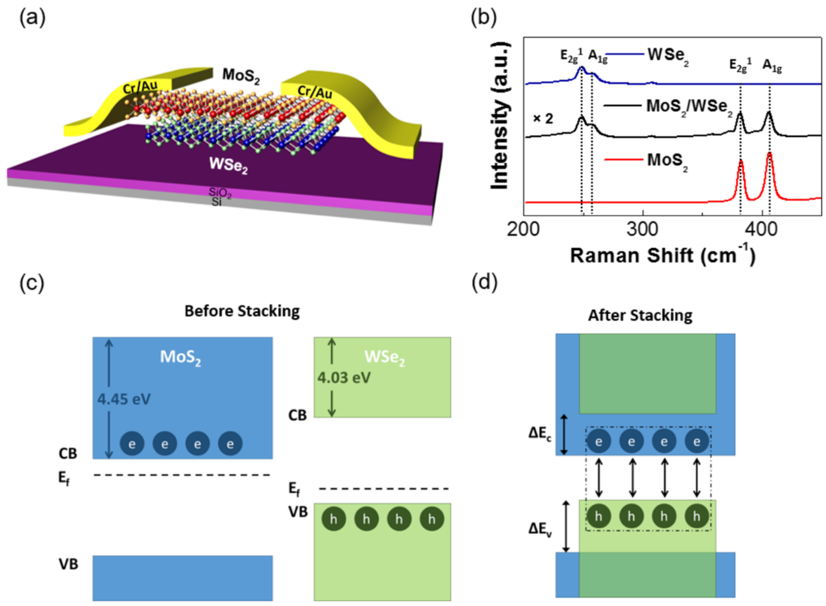

Figure 1. (a) Schematic diagram of dual channel MoS_2/WSe_2 heterostructure FET. (b) The Raman spectra of MoS_2, WSe_2, and overlapped MoS_2/WSe_2 regions. (c) The band diagram showing band structures of pristine MoS_2 and WSe_2 before stacking. (d) The band diagram of the MoS_2/WSe_2 heterostructure illustrating the formation of depletion region at heterointerface.

tunneling layer in between the metal and MoS_2 to form a metal−insulator−semiconductor (MIS) structure. This MIS structure can reduce the contact resistance by the optimum trade-off between the tunneling resistance of the insulating layers and the Schottky barrier lowering and the elimination of the interface states that arise from the direct contact between the metal and the semiconductor. Although mono- and bilayers of the hexagonal boron nitride (h-BN)/MoS_2 heterostructure demonstrate high-quality Ohmic contact, the requirement of a variety of heterostructure devices including negative differential resistance, ambipolar, tunneling, and photodevices demands other configurations as well, where the role of the insulating layer can be supplemented to add more functionalities to the devices, thus creating a diverse ecosystem of smart multifunctional integrated chips. In this scenario, we have proposed and demonstrated the application of a semiconducting bilayer of MoS_2 both as a tunneling and active channel in the heterostructure device, thus replacing the role of BN and enabling additional functionality in the device.

MoS_2/WSe_2 heterostructures have been widely studied because they offer a type-II band alignment having a heterointerface of a staggered gap which can be used for multiple optoelectronic and photovoltaic applications,[31,32] and in the current work, we have demonstrated a prototype of this heterostructure to access the individual channels in an unconventional way. This heterostructure device comprised of vertically stacked bilayer MoS_2 and few layered WSe_2 layers. Benefiting from the atomic scale thickness and different conduction regimes of MoS_2 and WSe_2, we have employed bilayer MoS_2 as a dielectric tunneling layer for WSe_2 as well as to achieve dual channel operation in the heterostructure device. Moreover, the use of MoS_2 as a tunneling layer has greatly reduced the contact resistance and Schottky barrier for WSe_2 contact.

2. RESULTS AND DISCUSSION

Figure 1a is the schematic diagram of dual channel MoS_2/WSe_2 heterostructure (DMW) field-effect transistor (FET) in which bilayer MoS_2 is stacked on a six-layer WSe_2. After stacking the layers, metal electrodes (Cr/Au) are deposited in such a way that only the top MoS_2 layer is in direct contact with metal electrodes. Figure 1b is the Raman spectra of MoS_2 and WSe_2 layers obtained using a 532 nm laser at room temperature. In the MoS_2 Raman spectrum, the presence of signature peaks: E^1_{2g} and A_{1g} at frequencies of 383 and 405 cm^{-1} confirms the flake to be MoS_2 and the difference of frequencies between E^1_{2g} and A_{1g} peak is 22 cm^{-1}, which implies the MoS_2 to be a bilayer.[33] The WSe_2 Raman spectrum comprises of signature WSe_2 peaks E^1_{2g} and A_{1g} and the difference between the peak frequencies indicate the WSe_2 thickness to be more than four layers.[34,35] The WSe_2 thickness is further confirmed by atomic force microscopy, which comes out to be 4.2 nm (six layers), as shown in Figure S1. The Raman spectrum of the overlapped region comprises of both MoS_2 and WSe_2 peaks, in which a significant decrease in the intensity of both MoS_2 and WSe_2 peaks is observed. This has been attributed to the quenching effect, where an additional recombination mechanism of the photogenerated electron−hole pairs at the heterointerface results in a significant drop in the spectrum intensity.[36]

Moreover, a blue shift in the MoS_2 peak in the overlapped region indicates p-type doping in MoS_2. This can be explained from the band alignment of the MoS_2/WSe_2 heterostructure which belongs to the type-II category as shown in Figure 1c, which subsequently leads to the transfer of electrons and holes to align the Fermi level across the type-II heterointerface.[15,37] This ultimately results in the formation of depletion region, in the respective layers (n-type MoS_2 and p-type WSe_2, such doping has been attributed to several factors like lattice defects, vacancies, impurities, etc.). The extent of this depletion region or charge transfer depends on various factors including intrinsic doping concentration, number of layers, and the quality of the MoS_2/WSe_2 heterointerface. Moreover, the observation of quenching, shift in the Raman spectra, and the charge transfer between the layers indicates strong coupling between MoS_2 and WSe_2 layers.

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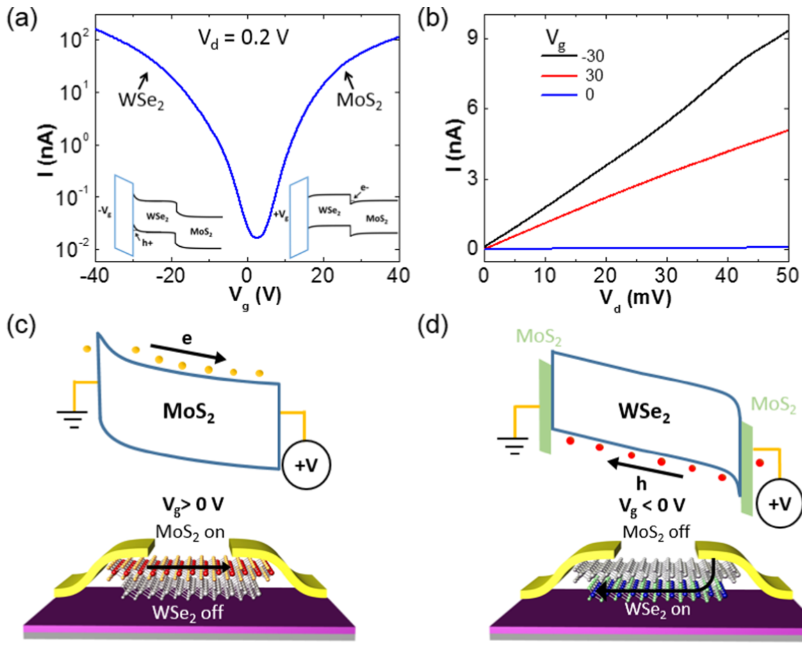

Figure 2. (a) Transfer characteristic curve of dual channel FET at $V_d = 0.2$ V in semi-logarithmic scale. (b) The output characteristic curve of dual channel FET at different back gate voltages. (c) Schematic band diagram and device schematic illustrating the band structure and current flow for positive V_g. (d) Schematic band diagram and device schematic illustrating the band structure and current flow for negative V_g.

Figure 2 illustrates the electrical characteristics of DMW FET. As discussed above, both MoS_2 and WSe_2 exhibit n-type and p-type behavior, respectively, which can be seen from their transfer characteristics as well.[15,37] However, the transfer characteristics of DMW FET exhibits an ambipolar transport with an on/off ratio of around 10^4 for both the positive and negative back gate voltage, as seen in Figure 2a. DMW has a minimum conductivity near zero back gate voltage due to the depletion region at the heterointerface of MoS_2 and WSe_2.[15,37] However, the conductivity of the device increases, when the back gate voltage is increased in either positive or negative directions. This is also reflected in the output characteristics as shown in Figure 2b, where the DMW has a minimum current at $V_g = 0$ V. Whereas, when the back gate is biased in positive or negative regime, the DMW exhibits linear characteristics, thus indicating the formation of Ohmic-like contacts. This observation of the ambipolar transport and the formation of Ohmic-like contacts to both the layers can be explained from Figure 2c,d. As discussed in the previous section, the transfer of MoS_2 over WSe_2 layers results in charge transfer and formation of depletion layer at the heterointerface. This results in an apparent charge neutrality in the heterostructure which can also be seen in the transfer characteristics (Figure 2a). As the gate sweeps to the positive regime (Figure 2c), the downward band bending under the influence of positive gate electric field results in electron accumulation in MoS_2 and further depletion of charge carriers in WSe_2 as also shown in the inset of Figure 2a. This results in an exponential rise in the current flowing through the MoS_2 channel through metal electrodes as can be seen in the transfer characteristics. Whereas during the negative gate regime, reverse band bending occurs due to the negative gate electric field which results in the accumulation of holes in WSe_2 and the formation of current channel. As there is no direct contact between WSe_2 and metal electrodes, the only possible way for carrier transport is tunneling through the intermediate MoS_2 layers from metal electrodes to the underlying WSe_2 as shown in Figure 2d. This explanation is further validated by the fact that in the negative gate regime, MoS_2 is fully depleted of carriers and acts like a dielectric tunneling layer, thus forming an MIS contact to the underneath WSe_2 active channel. Since one of the critical parameter of MIS contact is the barrier thickness, the tunneling probability across a barrier depends exponentially on the barrier width. Therefore, MoS_2 thickness is critically important for efficient injection of carriers into the channel. This is further evident from similar DMW devices with different MoS_2 thickness, as shown in Figure S2, and it can be seen that there is a remarkable decrease in carrier injection in WSe_2 even with a slight increase in MoS_2 thickness. The incorporation of the top layer in the DMW heterostructure device results in the dual channel transport through MIS contact formation without any additional metal contact engineering. In the next step, we further investigate the working of the MIS contact through electrical measurement at variable temperatures.

To evaluate the performance of the MIS contact, we performed the temperature-dependent measurement of our DMW FET in a temperature range of 250−370 K (step size: 20 K). According to thermionic theory, eq 1 can be used to describe the current in the device.[38−40]

$$I = AA^{*}T^{3/2}\exp\left(-\frac{e\varnothing_b}{k_B T}\right)\exp\left(\frac{eV_d}{k_B T} - 1\right) \tag{1}$$

In this equation, I is the current, A is the device area, A^* is the modified Richardson constant, $\varnothing_b$ is the Schottky barrier height (SBH), V_d is the applied drain voltage, e is the electron charge, k_B is the Boltzmann constant, and T is the temperature in Kelvin. We have measured the current as a function of temperature and extracted the SBH from the slope of the graph between $\ln(I_d/T^{3/2})$ and $1/T$ at a fixed drain bias (details in the Supporting Information). SBH was determined from the flat-band voltage, which is defined as the gate voltage at which the curve ceases to decrease linearly with the gate voltage.[30]

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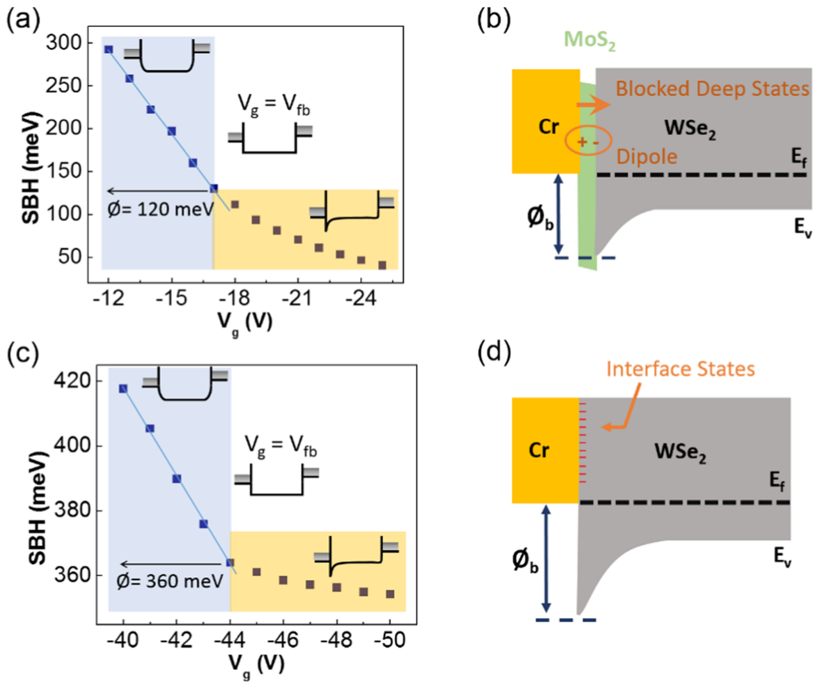

Figure 3. (a) Extracted Schottky barrier heights for WSe_2 at different back gate voltages (MIS contact). (b) Schematic band diagram for Cr and WSe_2 with MoS_2 tunneling contact (reduced Schottky barrier). (c) Extracted Schottky barrier heights for Cr contact with WSe_2 at different back gate voltages (MS contact). (d) Schematic band diagram for Cr/Au and WSe_2 contact (high Schottky barrier).

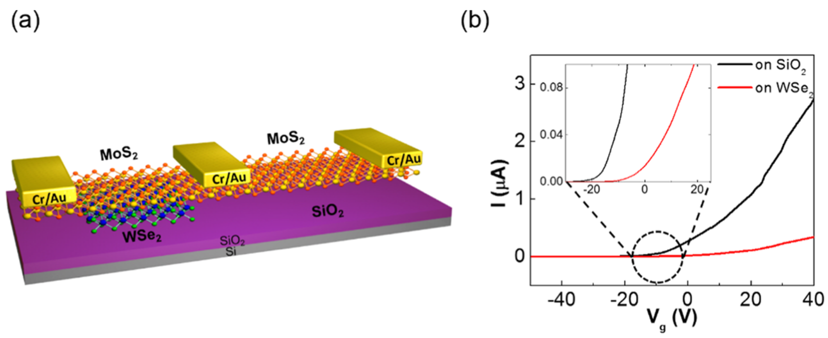

Figure 4. (a) Schematic illustration of the MoS_2/WSe_2 device. (b). Transfer characteristics of MoS_2 on the SiO_2 substrate and on WSe_2.

The value of the SBH comes out to be around 120 meV, as seen from Figure 3a. To compare the performance of the MIS contact with the metal−semiconductor (MS) contact, we fabricated the WSe_2 device with direct metal (Cr/Au) contacts. From the temperature-dependent measurement and using eq 1, SBH was extracted and is shown in Figure 3c. From $V_g = V_{FB}$, SBH comes out to be around 360 meV which is around 3 times higher than the SBH for the MIS contact.

This extreme reduction in the SBH can be explained by the Bardeen theory, which takes into consideration the effect of surface states at the metal−semiconductor interface. At the metal−semiconductor interface, besides surface states, interaction between the metal and semiconductor results in a high density of interface states, also known as metal-induced gap states, as shown in Figure 3d. These factors result in high SBH due to the Fermi-level pining effect. Furthermore, local inhomogeneities at the TMD's surface and metal-induced doping of TMDs are also known to cause Fermi-level pinning.[41,42] The effect of all these factors can be reduced by inserting an atomically thin dielectric layer between the metal and the semiconductor, which prevents the direct interaction between the metal and the semiconductor and therefore, results in reduced SBH as shown in Figure 3b. Another advantage of using the MIS structure is the formation of interfacial dipoles of opposite polarity at metal−insulator and insulator−semiconductor interfaces, which can neutralize each other and, thus, facilitate in further reduction of SBH.[29]

As high SBH is the main cause of high contact resistance which leads to detrimental device performance, this decrease in SBH should also result in a reduced contact resistance which is calculated and compared with the conventional metal electrodes. Here, we have calculated the contact resistance (R_c) of MIS contact using the Y-function method.[43−45] For comparison, three WSe_2-based devices were fabricated with Cr contacts and electrical characteristics of these devices are shown in Figure S4. The R_c value for Cr-WSe_2 contact for all three devices as calculated by the Y-method is of the order of 10^6 Ω μm, which is consistent with previously reported values of untreated metal−WSe_2 contacts.[24,46] The R_c value of the MIS contact in the DMW device is 80 kΩ μm, which is around 85 times better than the metal−WSe_2 contact and signifies the superiority of the MIS contact over the metal-semiconductor

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contact. However, this R_c value is higher than the reported values of 1.8 and 3 kΩ μm for MoS_2 MIS contacts.[29,30] SBH is one of the leading factor for high contact resistance and can be improved further by work function engineering of the contact metal.[29,30] Furthermore, process residues during transfer, fabrication, and metal deposition steps can limit the contact resistance improvement. Therefore, R_c can be further improved by using a cleaner transfer method followed by an ultra-high vacuum metal deposition.[47] As there is a considerable energy difference between the conduction and the valence band edge of MoS_2 and WSe_2, respectively, it is very challenging to form efficient electrical contacts to both the materials simultaneously. In the current work, simultaneous contacts to both MoS_2 and WSe_2 2D layers have been successfully achieved using direct metal−semiconductor (MS) and tunneling-based MIS contacts, respectively.

Besides contact resistance of the DMW device, it is important to identify the charge transport path when the device is operating in the tunneling MIS contact regime. For this purpose, we quantitatively evaluate the charge transfer between MoS_2 and WSe_2 layers using the device shown in Figure 4a. In this device, one-half of MoS_2 is on WSe_2 whereas another half is on the Si/SiO_2 substrate. Moreover, to avoid any tunneling current through MoS_2, the length of the WSe_2 layer is intentionally chosen such that it does not overlap with top metal contacts. Figure 4b provides a comparison between the transfer characteristics of MoS_2 on SiO_2 and WSe_2 and a clear shift of around 15.7 V is observed in the threshold voltage (see the Supporting Information for comparison and analysis[48] of hysteresis in the transfer characteristics of both FETs). The threshold voltage of MoS_2 on SiO_2 is −18.9 V, whereas the threshold voltage of MoS_2 on WSe_2 is −3.2 V indicating the charge transfer at the heterointerface. The depleted carrier density in MoS_2 is calculated to be 1.2×10^{12} cm^{-2} from the upshift of threshold voltage, using formula $n = e^{-1}C_g\Delta V_{th}$, where ΔV_{th} is the change in threshold voltage, $e = 1.6 \times 10^{-19}$ C and $C_g = 1.23 \times 10^{-8}$ F cm^{-2} for 300 nm SiO_2,[15,37] which is also reflected in the device current which decreases by almost three times in the WSe_2 channel overlapped device (Figure 4b). Moreover, it can be seen from Figure 4b that MoS_2 is in completely off state and does not conduct for $V_g < V_{th}$. This is further evident from the transfer characteristics of the other DMW devices (Supporting Information, Figure S2) where a consistent drop in the channel current in the negative gate regime is observed with increasing the top MoS_2 layer thickness. Therefore, it can be safely concluded that for DMW FET, the main current contribution in the negative V_g regime is from WSe_2 with MoS_2 acting as a tunneling dielectric in the MIS contact configuration.

3. CONCLUSIONS

To summarize, we have demonstrated the operation of a new heterostructure device where additional functionalities can be added to the device by switching the layer's type and thickness. In particular, we have illustrated the operation and working of dual channel FET in which a top bilayer MoS_2 was incorporated to act both as a channel as well as a tunneling layer to the bottom few layer WSe_2 of the heterostructure. For a positive gate voltage, WSe_2 is depleted of carriers whereas MoS_2 acts as the active channel layer. For the negative gate voltage, MoS_2 is depleted of carriers and acts as a tunneling layer to the underlying WSe_2 by forming an MIS contact. This MIS structure results in a highly reduced contact resistance of 80 kΩ μm and a SBH value of 120 meV. These results provide a promising approach to use diverse 2D materials to fabricate smart and multifunctional heterostructure devices for future nanoelectronics and optoelectronics applications.

4. EXPERIMENTAL METHODS

4.1. Device Fabrication. The MoS_2/WSe_2 heterostructure was fabricated using a conventional wet transfer method. In the first step, thin flakes of WSe_2 were exfoliated from the bulk crystal on a clean highly p-doped Si substrate capped with a 300 nm thick SiO_2 layer using the Scotch tape method. Then suitable flakes were selected by optical microscopy. For obtaining MoS_2 flakes to be stacked on the selected WSe_2 flake, MoS_2 flakes were exfoliated on the poly(methyl methacrylate) (PMMA)/poly(vinyl alcohol) (PVA)-coated Si substrate. PVA was later dissolved in water leaving behind MoS_2 on PMMA. The selected MoS_2 flake was picked up and transferred on top of WSe_2 using the aligned transfer system which is fitted with an optical microscope. After the transfer, the device was annealed at 100 °C for 1 h in an Ar environment to enhance interfacial coupling between MoS_2 and WSe_2. Electrodes were patterned using e-beam lithography followed by metal deposition (Cr/Au 10:30 nm) in an electron-beam deposition chamber.

4.2. Device Characterization. Raman spectroscopy was performed to characterize the flakes using a 532 nm laser under ambient conditions. Electrical characterization of the device was performed under vacuum in a dark environment using a Keithley 4200-SCS parameter analyzer.

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acsami.8b05549.

AFM height profile, transfer characteristics with different MoS_2 thickness, details of Schottky barrier height extraction, details of the Y-function method, and electrical characteristics of WSe_2 devices with metal contact (PDF)

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Notes

The authors declare no competing financial interest.

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