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Dual-Channel WS_2/WSe_2 Heterostructure with Tunable Graphene Electrodes

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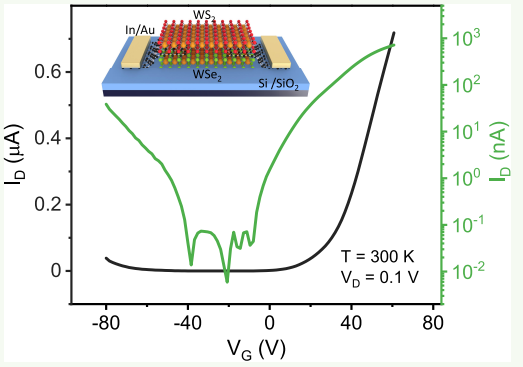
ABSTRACT: Two-dimensional semiconductor heterostructures provide significant research potential for electronic and optoelectronic applications because of their scaled thickness, pristine heterostructure interface, and ultrafast carrier transport. Herein, we report a dual-channel field-effect transistor based on n-type WS_2 and p-type WSe_2 layered heterostructure using multilayered graphene as electrodes to enable electron-dominated ambipolar electrical transport. WS_2 exhibits mobility of 20 $cm^2\ V^{-1}\ s^{-1}$ and an on/off ratio of 10^5, whereas WSe_2 exhibits mobility of 5 $cm^2\ V^{-1}\ s^{-1}$ and an on/off ratio of 10^4. Furthermore, our results show negative Schottky barrier heights between dual-channel heterostructure and multilayered graphene. The proposed design reduces complications in the fabrication of devices with integrated heterostructures, particularly for complementary metal-oxide semiconductor inverter applications.



KEYWORDS: *graphene electrode, dual channel, gate tunable, WSe_2, WS_2*

INTRODUCTION

Because the two-dimensional (2D) heterostructures have atomic-scale thickness and transparency, their integration technology has enabled the development of highly advanced electronic applications. These applications include tunable p−n junction diodes and high-mobility field-effect transistors (FETs);[1−3] graphene used for transparent electrodes owing to its true 2D and gap-free properties;[4−6] other transition metals, such as tungsten disulfide (WS_2) and tungsten diselenide (WSe_2), which possess adequate energy band gap; free dangling bond dichalcogenide (TMD) materials; and smooth surfaces.[7−10] These features are effective in forming lateral and vertically stacked van der Waals heterostructures for high-performance and low-power electronic applications. Therefore, several TMD materials and their double-layer channel heterostructures are remarkably effective options for dual-channel transistors[11−13] based on p−n junction operation.[14,15] Notwithstanding the development of various ohmic contact technologies, such as deposition of metal electrodes under ultrahigh vacuum,[16] transfer of thin metal films onto 2D semiconductors,[17] and few-layered mechanically exfoliated h-BN[18] on top of 2D semiconductors, many researchers are continuing their attempts to improve the ohmic of TMD materials. Fundamental and application studies using quantum properties in the low-temperature region are known to develop a problem in terms of ohmic contact. This is because the tunneling barrier of electrons or holes passing through the Schottky barrier is large. High-performance heterostructures rely primarily on p−n junctions and low-resistance ohmic contacts. Various techniques, such as graphene electrodes, doping, and tunneling effects, have been employed in this domain.[19−22] Among these, application with graphene electrodes has been reported to benefit primarily from the constraints of higher mobility, low or negative Schottky barrier heights (SBHs), and lattice mismatch.[23,24]

In this study, we developed the dual-channel WS_2/WSe_2 heterostructure with graphene contacts (DWWG). It can be applied as a reducing metal contact to semiconductors. To obtain a low barrier and prevent lattice mismatch, we used a few-layer graphene as electrodes for the WS_2/WSe_2 heterostructure. It is noteworthy that we achieved negative SBH as well as a high on/off ratio on both p- and n-type. WS_2 exhibited mobility of 20 $cm^2\ V^{-1}\ s^{-1}$ and an on/off ratio of 10^5, whereas WSe_2 exhibited mobility of 5 $cm^2\ V^{-1}\ s^{-1}$ and an on/off ratio of 10^4. The electron-dominated ambipolar behavior of our device, wherein electrons and holes transport could be modulated by the gate bias (herein, the graphene electrodes come in contact with the dual-channel heterostructure), exhibited negative SBH. In addition, dual-channel characteristics with both n- and p-type properties were exhibited. This dual-channel structure can be applied to CMOS logic circuits through selective carrier transport to minimize fabrication complexities.[11,13,25] In

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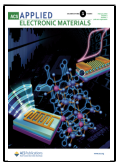

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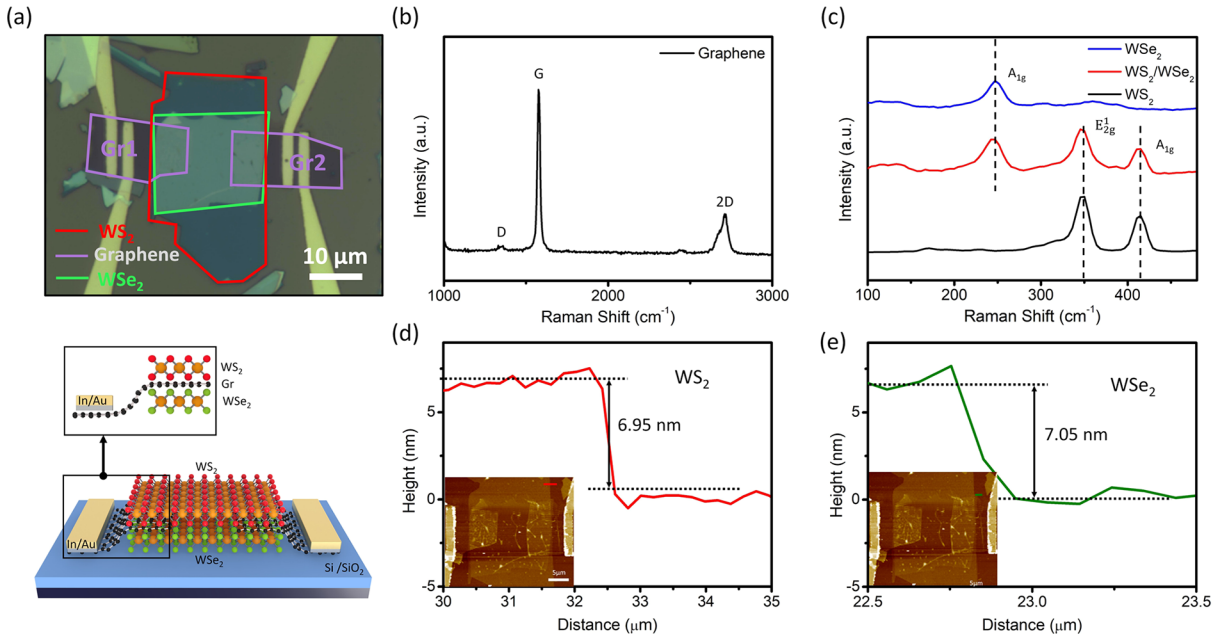

Figure 1. (a) Optical microscopy image and schematic of the DWWG device showing the WS_2 at the top, WSe_2 at the bottom, and graphene between the heterostructure as electrodes. (b) Raman spectrum of few-layer good quality graphene used as DWWG device electrode. (c) Raman spectrum of few-layer WS_2, WSe_2, and WS_2/WSe_2 heterostructures. (d) AFM image and thickness of WS_2. (e) AFM image and thickness of WSe_2.

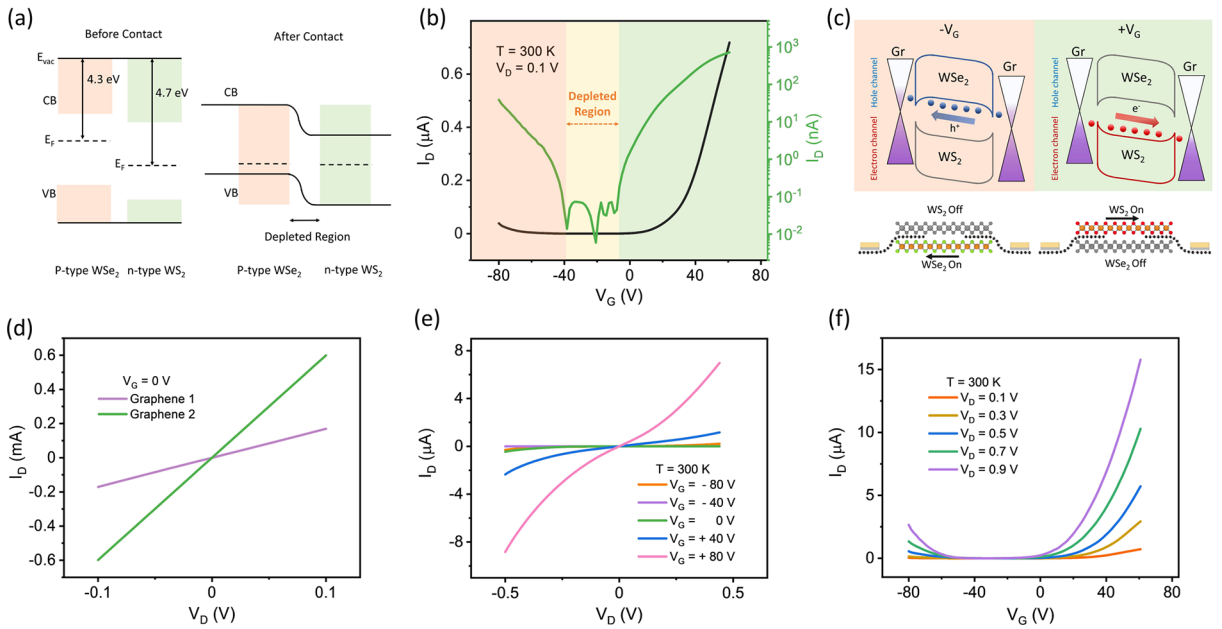

Figure 2. (a) Energy band diagram of WS_2 (n-type) and WSe_2 (p-type) before and after contact with a formation of depletion. (b) I_D–V_G characteristics of DWWG device revealing electron-dominated ambipolar characteristics with depletion region. (c) Lateral band diagrams and schematic of DWWG device illustrating the band structure and current flow at positive (WS_2 on) and negative (WSe_2 on) V_G. (d) I_D–V_D characteristics of each graphene contact at zero gate voltage revealing ohmic properties at a drain voltage of 0.1. (e) I_D–V_D characteristics of DWWG device at different gate voltages. (f) I_D–V_G characteristics of DWWG device at different drain voltages.

addition, depending on the drain voltage, the depletion region can be modulated for the off-state in transistors.

RESULTS AND DISCUSSION

Figure 1a shows an optical microscopy image and schematic of the dual-channel WS_2/WSe_2 heterostructure with graphene electrode FET. After the dry transfer of two graphenes on each edge of the seven-layer WS_2, the seven-layer WSe_2 was stacked on top. Finally, a metal electrode (In/Au) was deposited on the graphene (Figure S1). The Raman spectra of the graphene electrodes and the WS_2 and WSe_2 layers were verified using a laser of wavelength 532 nm at room temperature. Graphene exhibited a typical Raman spectrum with D, G, and 2D peaks. Here, the low D peak revealed the good quality of the graphene (Figure 1b).[26,27] In the Raman spectra, the presence of Raman peaks and A_{1g} at the frequencies of 350 and 415 cm^{-1} in WS_2 indicates that the exfoliated flake was WS_2 (Figure 1c).[11,28,29] Similarly, WSe_2 can be distinguished as corresponding to A_{1g} at

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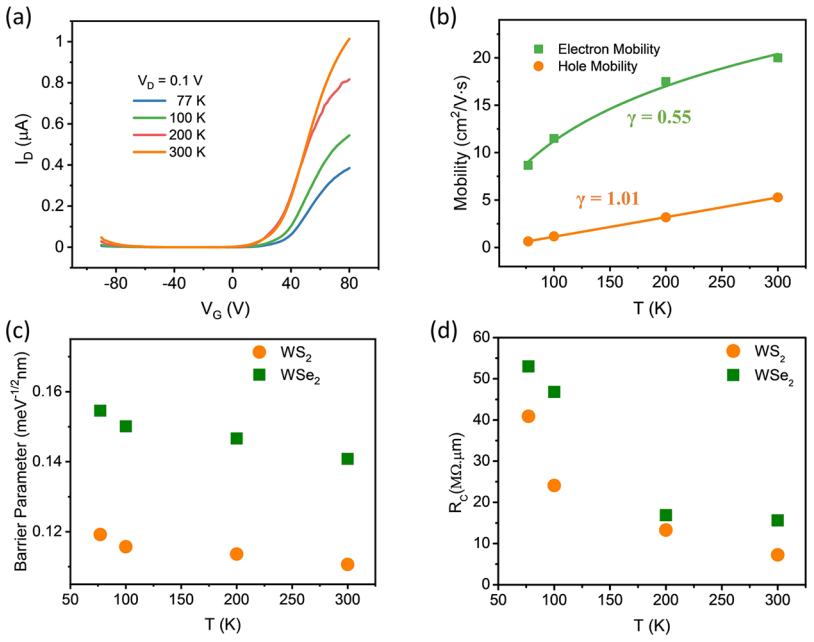

Figure 3. (a) I_D-V_G characteristics of DWWG device concerning temperature illustrating electron-dominated ambipolar characteristics with a drain voltage of 0.1 V. (b) Variation in electron and hole mobility of DWWG device for temperatures in the range 77−300 K. (c) Temperature-dependent barrier parameter for DWWG device in the temperature range of 77−300 K. (d) Contact resistance of the DWWG device in the temperature range of 77−300 K using the Y-function method.

~250 cm^{-1}.[12,30,31] The Raman peaks in the overlapped WS_2/WSe_2 region reveal a reduction in intensity.[11−13]

Atomic force microscopy (AFM) measurements on the highlighted red line on WS_2 flakes and highlighted green line on WSe_2 flakes verify the thicknesses of the WS_2 and WSe_2 flakes (Figure 1d,e), respectively. The thickness of the WS_2 and WSe_2 flakes was 6.95 and 7.05 nm, respectively. This indicates that each flake had seven layers.[28,31]

The work function of n-type WS_2 and p-type WSe_2 were 4.7 and 4.3 eV, respectively (Figure 2a).[32,33] The n-type WS_2 layer diffused electrons to the p-type WSe_2 layer, whereas the p-type WSe_2 layer diffused holes to the n-type WS_2 layer. This phenomenon occurred until the electric field generated by diffusion was in equilibrium with the electric field. Thereby, the depletion region was formed at the n-WS_2/p-WSe_2 interface. It was verified that this depletion layer was formed at a low drain voltage. It did not exist at a high voltage because electrons have adequate energy to pass through it. The low potential barrier was achieved for p-type WSe_2 and n-type WS_2 using graphene electrodes.[11−13] Conventional, low-work-function metals are favorable for n-type materials because a Fermi level of low-work-function metals is developed near the conduction band of 2D materials, which enables electron injection.[34,35] Conversely, the Fermi level with a high work function formed near the valence band of n-type materials would obstruct the electron streaming. Consequently, low-work-function metals are suitable for n-type materials, whereas high-work-function metals are suitable for p-type materials.[36] We incorporated two graphene electrodes in our heterostructure. This formed the low barrier for n-type WS_2 and p-type WSe_2. A negative SBH was observed in both n-type and p-type channels owing to this barrier degradation.

The I_D-V_G characteristics of the DWWG heterostructure using graphene contact for dual-channel FET are illustrated in Figure 2b. Zhu et al. reported black phosphorus FETs with electron-dominated ambipolar characteristics. However, they have a narrow off-current area, which makes them unsuitable for digital integrated applications that require a large off-state screen.[13,37] In contrast, our DWWG heterostructure provides a large off-state screen area of ~40 V and modulated off-state screen (Figure S2). Hence, it can be more effective for logic circuit applications.

The proposed DWWG heterostructure exhibits electron-dominated ambipolar behavior owing to the electron transport in the WS_2 channel and hole transport in the WSe_2 channel (Figure 2c).[13] The band bends downward because of the positive gate electric field, which accumulates electrons in WS_2 and subsequently causes charge-carrier depletion in WSe_2.[12,13] In contrast, the negative gate electric field shows reverse band bending, wherein holes are accumulated in WSe_2, and a current channel is formed.[13] The WSe_2 layer causes charge transfer and the formation of a depletion layer at the heterogeneous interface. This results in apparent charge neutrality in the heterostructure. The band bends downward when the gate sweeps in the positive direction. This promotes electron accumulation in WS_2 and further charge-carrier depletion in WSe_2.[12,13]

Figure 2e,f shows the I_D-V_D and I_D-V_G characteristics of the DWWG heterostructure and illustrate the electron-dominated ambipolar transport under different voltage bias and apparent low Schottky barrier under different drain bias at 300 K. Two graphene electrode contacts exhibited good ohmic contact (Figure 2d) and in the plot of I_D-V_G characteristics, their Dirac points are shifted at −21.6 and 12 V, respectively (Figure S3). A Dirac peak shift is caused by the adsorption and desorption of environmental gases; however, the amounts of the shifts vary depending on the fabrication process. When graphene is pristine and undoped, its Dirac point is normally located at zero gate voltage. Positive and negative shifts in the Dirac point can occur due to donors and acceptors. Physical adsorption of oxygen and water molecules on SiO_2 or graphene surfaces can disturb the electron−hole concentration under ambient conditions. Additional dopants existing in air, such as oxygen and nitrogen, can act as electron acceptors by adsorbing weakly to graphene.[38,39]

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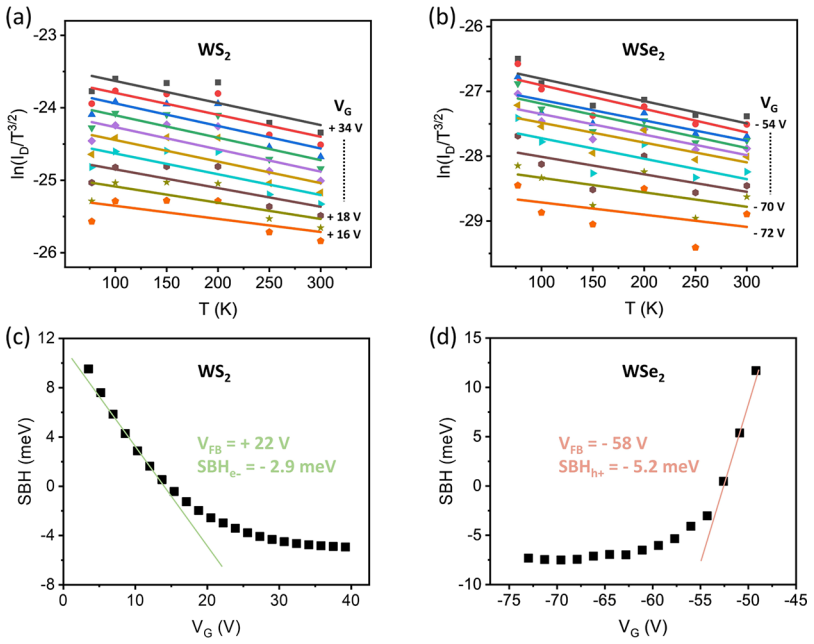

Figure 4. (a) Arrhenius plot of n-type WS_2 as a function of gate voltage (V_G = +16 to +34 V) illustrates the variation in slope in the temperature range 77−300 K. (b) Arrhenius plot of p-type WSe_2 as a function of gate voltage (V_G = −54 to 72 V) illustrates the variation in slope in the temperature range 77−300 K. (c) Dependence of SBH of n-type WS_2 on the gate voltage. (d) Dependence of SBH of p-type WSe_2 on the gate voltage.

The performance of the DWWG heterostructure was investigated by temperature-dependent transport measurement in the range of 77−300 K (Figure 3a). The significant decrease in current implied that the reduction in charge-carrier was related to a decrease in thermal energy. Figure S4a,b shows the I_D−V_D characteristics as a function of temperature at a fixed V_G of 40 V (WS_2 on) and −80 V (WSe_2 on), respectively, in the temperature range of 77−300 K. Both WS_2 and WSe_2 exhibited increased SBH as the temperature decreased to 77 K. This could be attributed to the use of the same graphene contact on both the channel, rather than using metal contacts. The graphene contact to a dual channel is an optimum contact to drain and source and is tunable due to the lower density of states compared to that of the metals. It can also be assumed that this deviation comes due to the presence of inhomogeneities, which might be intrinsic (defects) or extrinsic (contamination in fabrication) (Figure 3b).

The field-effect mobilities of holes and electrons in a DWWG heterostructure FET with graphene contact were computed as follows

$$\mu = \frac{L}{W}\left(\frac{dI_D}{dV_G}\right)\left(\frac{1}{C_i \times V_D}\right) \quad (1)$$

where L is the length of the device, W is the width, I_D is the source−drain current, V_G is the gate bias voltage, C_{ox} is the capacitance of the 285 nm thick SiO_2, and V_D is the drain voltage. The mobilities for the WS_2 and WSe_2 channels at 300 K were determined as 20 and 5 $cm^2\ V^{-1}\ s^{-1}$, respectively. Here, mobility shows a strong temperature dependence and variation in the dual-channel DWWG heterostructure device due to the higher content of grain boundaries and impurity scattering. We think that at low temperatures, the ionized impurity scattering is more dominant and limits the mobilities.

This can be expressed by the power-law $\mu_{FE} \approx T^{\gamma}$, which indicates the difference in carrier transport. In our device, both channels exhibit consistent dependence on temperature. Furthermore, the values of γ were determined to be 0.55 and 1.01.

We applied the direct tunneling (DT) and Fowler−Nordheim (F−N) tunneling models to further investigate the transport properties of the seven-layer WS_2 and WSe_2 across graphene contacts. Notwithstanding the thermionic emission process, it is predicted that electrons would be thermally compelled to overcome the Schottky barrier. However, DT is more prevalent at lower temperatures for an ultrathin barrier. The triangular shape of the barrier enables electrons to tunnel through F−N. This is observed primarily at a high bias. The DT can be expressed as the following equation[40]

$$I_D = \frac{Aq^2V\sqrt{2m^*\Phi_B}}{h^2 d}\exp\left(\frac{4\pi d\sqrt{2m^*\Phi_B}}{h}\right) \quad (2)$$

where A is the electrical contact area, d is the barrier width, h is Plank's constant, m^* is the effective mass of an electron in the WS_2 (0.33 m_0) flake and a hole in the WSe_2 flake (0.46 m_0), and SBH is given by Φ_B.

F−N tunneling is expressed as[41,42]

$$I_D = \frac{Aq^3m_0V^2}{8\pi h\Phi_B d^2 m^*}\exp\left(-\frac{8\pi d\sqrt{2m^*}\,\Phi_B^{3/2}}{3hqV}\right) \quad (3)$$

A logarithmic behavior is exhibited by all the contacts, which indicates the significance of DT in our device. Thus, a plot of $\ln(I_D/V_D^2)$ as a function of $\ln(1/V_D)$ reveals a linear relationship (Figure S4c,d). F−N tunneling disappears because it is dominated at a higher bias. Therefore, eq 3 yields the barrier parameter $d\sqrt{\Phi_B}$ from the fitting equation for DT. Figure 3c shows the tunneling barrier heights in our device when the temperature was decreased from 300 to 77 K for each channel with graphene contacts and was calculated to be in the ranges of 0.11−0.12 and 0.14−0.54 $meV^{-1/2}$ nm for each WS_2/graphene contact and WSe_2/graphene contact, receptively. Essentially, the

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ACS Appl. Electron. Mater. 2023, 5, 913−919

barrier parameter for a WS_2/graphene contact is lower in our device.

The contact resistance in DWWG was analyzed using the Y-function (Ghibaudo) approach to explain the variation in contact resistance. Two-terminal electrical measurements were used to estimate the contact resistance, which strongly depends on the temperature (Figure 3d).[11,43,44] The Schottky barrier dominates the contact resistance in metal connections. Additionally, using a graphene contact as a tunneling layer can reduce the SBH while maintaining a low tunneling resistance.[4,6,45]

The current in the device is expressed as follows by applying the thermionic emission theory[44,46−48]

$$I = AA^* \times T^{3/2} \exp\left(-\frac{e\Phi_B}{k_B T}\right) \exp\left(\frac{eV_B}{k_B T} - 1\right) \quad (4)$$

where I represent the current, A^* is the modified Richardson constant, A is the device area, Φ_B represents SBH, V_D is the drain voltage, e is the electron charge, k_B is the Boltzmann constant, and T is the temperature in units of K. The SBH and Φ_B obtained using this equation are not equivalent to those of the conventional Gr−semiconductor junctions. The generation of the Schottky barrier in metal/semiconductor systems has not been understood well. The SBH is generally governed by the semiconductor surface states and the metalwork functions. To obtain the SBH, the reciprocal temperature dependence $\ln(I_D/T^{3/2})$ fit curves were plotted at different gate biases at the interface between the DWWG heterostructure FET and graphene contact (Figure 4a,b). The effective SBH in eV can be determined from the slope of these lines corresponding to the gate bias, V_{GS}. For $V_{GS} \leq V_{FB}$, the Schottky barrier obtained in Figure 4c,d corresponds linearly to V_{GS}. Thereby, the correct negative SBH values −2.9 meV for WS_2 and −5.2 meV for WSe_2 are achieved for devices under flat band voltage conditions +22 and −58 V, respectively. The observation reveals a decreasing trend of SBH, which is more dominant in hole transport.[23,24] The Dirac cone structure of graphene enables gradual charge-carrier doping in the dual-channel heterostructure through electrical bias. This results in a continual shift in Fermi levels, which enables the tuning of SBH and the modulation of charge-carrier injection in capable device switching[6,7,9] In addition, we studied the optical properties by illuminating our device at a range of light power (dark-field to 0.88 mW) using a 520 nm laser and plotting the I_D-V_D curve (Figure S5). The potential capability was determined for the graphene electrode hetero-junction based primarily on 2D materials to design novel heterostructures for digital and optoelectronic devices.[49,50]

CONCLUSIONS

In conclusion, we fabricated a dual-channel WS_2/WSe_2 heterostructure bipolar FET with graphene electrodes as junctions whose electron transport properties were investigated at temperatures ranging from room temperature to liquid-nitrogen temperature. The bipolar behavior of our device (wherein electron and hole transport can be modulated by the gate bias) exhibited a negative SBH when the graphene electrode was in contact with the dual-channel heterostructure. The proposed design is likely to contribute to the development of future integration applications that are functional at room and low temperatures for fundamental and application research of various heterostructures while minimizing ohmic problems and reducing the complexity of device fabrication.

EXPERIMENTAL SECTION

Growing WS_2 Crystal Using the Flux Method. The flux method was used to grow high-purity WS_2 crystals with tin (Sn) as the flux material. The flux material has a low melting point and helps dissolve solute in it for the chemical reaction. Subsequently, it was removed from the crystals by centrifuging the hot ampoule as soon as it is removed from the furnace (without permitting it to cool down). The source materials W (Sigma-Aldrich purity 99.99%), S (Sigma-Aldrich purity 99.99%), and Sn (Sigma-Aldrich purity 99.99%) were mixed in a particular ratio in an alumina crucible. Subsequently, the crucible was placed inside the quartz ampoule in an argon (Ar) environment in a glovebox. A cylinder made of high-purity (99.99%) SiO_2 quartz wool with remarkable insulation performance was loaded 1 cm above the alumina crucible to absorb excessive solvent during centrifuging. After being vacuumed and sealed, the ampoule was placed inside a high-temperature furnace at 1150 °C (with a rate of increase of 50 °C h^{-1}). The dwelling time was 36 h. Then, a cooling rate of 2.5 °C h^{-1} was adopted to attain 1000 °C. The resultant ampule was centrifuged. Finally, the grown crystals were used for device fabrication.

Growing WSe_2 Crystals Using the Flux Method. The flux method was used to grow high-purity WSe_2 crystals, wherein Se was used as a self-flux material. The flux material has a low melting point and helps dissolve the solute in it for the chemical reaction. In addition, it could be removed conveniently from the crystals by centrifuging a hot ampoule immediately after being removed from the furnace (without permitting it to cool down). The source materials W and Se (Alfa Aesar purity 99.999%) were measured and mixed in an alumina crucible, which was subsequently loaded in a quartz ampule in an Ar environment inside the glovebox. A cylinder made of high-purity (99.99%) SiO_2 quartz wool with remarkable insulation performance was loaded 1 cm above the alumina crucible to absorb excessive solvent during centrifuging. After being vacuumed and sealed, the ampoule was placed in a high-temperature furnace at 1100 °C (a ramp-up rate of 50 °C h^{-1}). The dwelling time was fixed at 48 h. Subsequently, the ampoule was cooled to 450 °C at a rate of 2.5 °C h^{-1}. The resulting ampule was centrifuged at 2000 rpm for 60 s. Finally, the crystals were analyzed by X-ray diffraction techniques and Raman spectroscopy to evaluate their formation and quality.

Fabrication of the DWWG Device. Using a typical Scotch tape approach, bulk n-type WS_2, p-type WSe_2 crystal, and graphite were employed for exfoliation on a precleaned and substantially p-doped Si substrate covered by a 285 nm thick SiO_2 layer. Next, optical microscopy was used to identify few-layer flakes. The dry transfer method was used to stack a suitable few-layer WS_2, WSe_2, and graphene. A poly(dimethylsiloxane) base substrate with a polycarbonate (PC) sacrificial layer was employed to pick up the few-layer WS_2 and graphene flakes. Then, the graphene electrodes were picked up using van der Waals forces from a WS_2 flake connected to the PC layer. Finally, the WS_2 flake with two graphene electrodes was released on the targeted WSe_2 flake in the glovebox filled with Ar gas. The remaining PC was removed by soaking the sample in chloroform for 30 min and drying it with nitrogen. The electrodes were created using electron-beam lithography after the transfer, followed by In (10 nm)/Au (30 nm) metal deposition in an electron-beam deposition chamber. Finally, annealing was performed at 150 °C for 3 h in a high-vacuum condition (10^{-6} Torr).

Characterizations of the DWWG Device. AFM was used to determine the thickness of the WS_2, WSe_2, and graphene flakes. A 532 nm laser was used under ambient conditions to characterize the flakes using Raman spectroscopy. A Keithley 4200-SCS parameter analyzer was used to perform electrical characterization of the device in a vacuum in a dark environment.

Electrical Measurement with Laser Illumination. Two-terminal measurement was performed at room temperature and liquid-nitrogen temperature to characterize the electrical properties of FETs. The device was illuminated by laser light with a power density of 1 mW cm^{-2} and wavelength of 520 nm to observe the photoresponse.

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ACS Appl. Electron. Mater. 2023, 5, 913−919

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsaelm.2c01465.

Description of fabrication steps, additional experimental data on photoresponse, details of the Y-function method, electrical characteristics of WS_2, WSe_2, and graphene electrodes (PDF)

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Author Contributions

H.K., J.K., and N.A.N.P. performed fabrication, temperature-dependent electrical measurements, and data analysis. H.K. performed the Raman and AFM characterization. I.U. grew the WS_2 and WSe_2 crystals using the self-flux method. D.W. contributed to the revision of the manuscript. G.-H.K. conceived the projects and supervised the tasks from fabrication to data analysis and manuscript writing. All authors have approved the final version of the manuscript

Notes

The authors declare no competing financial interest.

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