Transient Response of h-BN-Encapsulated Graphene Transistors: Signatures of Self-Heating and Hot-Carrier Trapping

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ABSTRACT: We use transient electrical measurements to investigate the details of self-heating and charge trapping in graphene transistors encapsulated in hexagonal boron nitride (h-BN) and operated under strongly nonequilibrium conditions. Relative to more standard devices fabricated on SiO$_2$ substrates, encapsulation is shown to lead to an enhanced immunity to charge trapping, the influence of which is only apparent under the combined influence of strong gate and drain electric fields. Although the precise source of the trapping remains to be determined, one possibility is that the strong gate field may lower the barriers associated with native defects in the h-BN, allowing them to mediate the capture of energetic carriers from the graphene channel. Self-heating in these devices is identified through the observation of time-dependent variations of the current in graphene and is found to be described by a time constant consistent with expectations for nonequilibrium phonon conduction into the dielectric layers of the device. Overall, our results suggest that h-BN-encapsulated graphene devices provide an excellent system for implementations in which operation under strongly nonequilibrium conditions is desired.
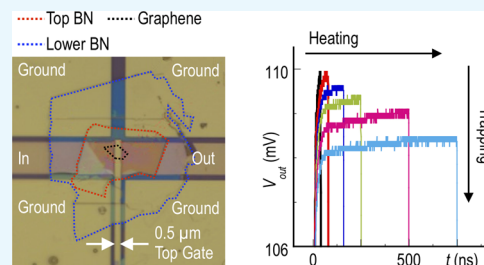
INTRODUCTION

The capacity to implement layered heterostructures by stacking different combinations of atomically flat materials has opened up new opportunities in recent years for the realization of various functional devices.[1] One of the primary examples of such a "van der Waals heterostructure" is provided by the graphene/h-BN system in which a conductive graphene sheet is sandwiched between layers of hexagonal boron nitride (h-BN).[2−6] A schematic illustration of this system is shown in Figure 1a, which indicates the main components of a field-effect transistor (FET) that is formed by encapsulating a thin graphene sheet (green) between two thicker layers of h-BN (blue). (Also indicated in this figure is an equivalent thermal circuit that we will use later on to analyze the transient dynamics of heating in such devices.) Hexagonal boron nitride is a wide-gap semiconductor with an indirect gap of ~6 eV[7] and a number of properties that make it compatible for integration with graphene. It is easily realized in atomically flat

form and has a honeycomb crystal structure that is well matched (~1.5% mismatch) to that of graphene.[8] It is not plagued by the interfacial dangling bonds or the bulk oxide traps, which tend to be present in SiO$_2$ and which are the source of hysteretic operation and hot-carrier trapping in graphene-on-SiO$_2$ devices. Finally, the thermal conductivity of h-BN is about 20 times larger than that of SiO$_2$, allowing it to function as an efficient heat sink in graphene/h-BN heterostructures.[8]

van der Waals heterostructures composed of graphene and h-BN have recently become popular for the investigation of exotic condensed-matter phenomena manifested at low temperatures (~1 K) where the suppression of electron−phonon scattering allows very high carrier mobilities [>10^5
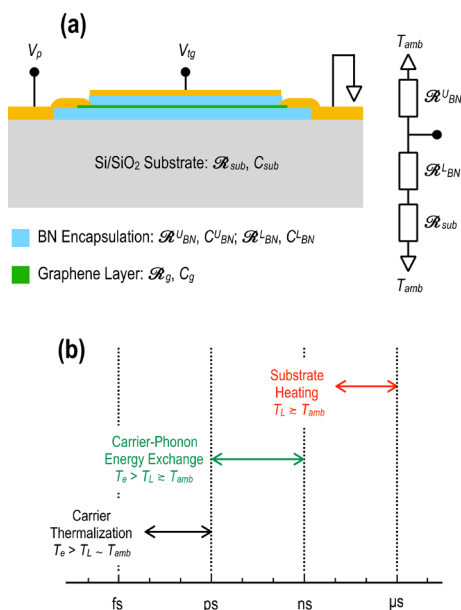
Figure 1. (a) Schematic illustration of the structure of the graphene/h-BN heterostructured FETs investigated here. The significance of the different thermal resistances ($\mathcal{R}$) and capacitances (C) is discussed in the main text. On the right of the image, we show a thermal-resistance model that can be used to address self-heating in these FETs. Superscripts "U" and "L" denote the upper and lower layers of h-BN, respectively, while "sub" refers to the SiO$_2$/Si substrate. (b) Representation of the different energy-exchange processes that are expected to arise in these devices when they are subjected to a large electric field. The horizontal scale represents time following the turn-on of the electric field that, for the purpose of discussion, is assumed to occur instantaneously (at time $t = 0$).

cm^2/(V·s)] to be achieved.[9−13] Far fewer studies,[14−16] in contrast, have addressed the nature of hot-carrier transport in these structures, in spite of the fact that this transport is most pertinent to active-device applications. It is this problem we explore in this research article in which we apply pulsed electrical measurements to determine the dynamics of energy transfer in graphene/h-BN FETs. The key result we demonstrate is significant immunity of transistor action to hot-carrier trapping, providing a marked improvement over graphene-on-SiO$_2$ devices, whose operation is known to be negatively impacted by such trapping at high fields.[17−23] We also identify the dynamics of self-heating in the graphene/h-

BN devices and discuss how this influences transistor performance. Overall, our results establish the excellent immunity of the graphene/h-BN system to hot-carrier degradation and highlight its value as a specific materials combination for the realization of active devices.

Before describing the results of our study, it is worthwhile first clarifying the different hot-carrier phenomena that can arise when graphene FETs are subjected to a large driving electric field. These phenomena are represented in Figure 1b, along with the various timescales on which they are expected to develop. The key subcomponents of the system here are the mobile carriers and phonons of the graphene layer and the phonons of the insulating h-BN and of the supporting (SiO$_2$/Si) substrate. Prior to turning on the electric field, these various subsystems can be assumed to be in thermal equilibrium at a common ambient temperature ($T_{amb} = T_e = T_L$, where T_e is the carrier temperature in graphene and T_L is the lattice temperature in the various layers). Once the field is applied, the carriers first thermalize at an effective "hot" temperature ($T_e > T_L = T_{amb}$) in a process involving a combination of Auger scattering and band-to-band recombination. As indicated in Figure 1b, the characteristic time associated with this thermalization ranges from tens of femtoseconds to a few picoseconds.[24] Following this, there is a slower exchange of energy from the hot carriers to the intrinsic phonons of graphene on an "energy-relaxation time" that may vary from picoseconds to nanoseconds, dependent upon temperature and carrier concentration.[25] While both the carrier thermalization and the subsequent electron−phonon energy exchange are "internal" to the graphene, further time-dependent character arises from the exchange of energy between the graphene and the surrounding dielectric layers.[26,27] This much slower process (commonly referred to as "self-heating") is not instantaneous but is governed instead by the thermal resistance of these layers ($\mathcal{R}$, including the interfacial resistance that arises from phonon mismatch between the layers[28]) and their associated thermal capacities (C). Thermal-transport simulations,[26] performed for graphene-on-SiO$_2$, have shown that this process may take as long as hundreds of nanoseconds before the system reaches full steady state. With this state achieved, the carrier temperature (T_e) in graphene may easily exceed 1000 K,[28] while the lattice temperature in the dielectric layers rises by hundreds of kelvin above ambient temperature ($T_L \gg T_{amb}$).[26]

Added to the role of the heating processes described above is the influence of carrier trapping. As noted already, this is
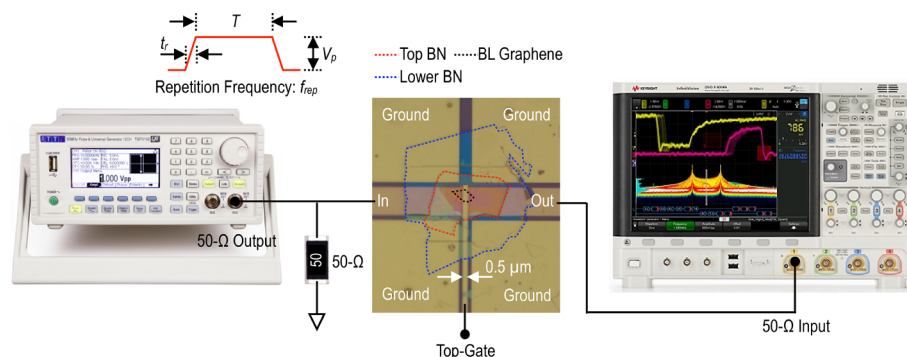

Figure 2. Schematic illustration of the pulsed-measurement scheme. The optical micrograph shows the active region of the device, outlining the lower (blue dotted line) and upper (red dotted line) h-BN flakes that encapsulate a small flake of bilayer graphene (black dotted line). The source−drain separation in this device is 0.5 μm.

known to be especially problematic for graphene-on-SiO$_2$ devices, due to a preponderance of possible trapping sites in the oxide system. In this research article, we make use of time-resolved electrical measurements to demonstrate that the graphene/h-BN system exhibits significantly enhanced immunity to carrier trapping relative to graphene-on-SiO$_2$ devices. This can be traced directly to the reduced presence of trapping centers in the insulating h-BN.

■ RESULTS

In this study, we use a rapid-pulsing approach[17,18] to investigate (at room temperature) the hot-carrier action in h-BN-encapsulated graphene FETs, comparing this with the corresponding behavior exhibited by graphene-on-SiO$_2$ devices. A full description of these devices and of the different measurement techniques used to characterize them is given in the Methods section at the end of this article. In the h-BN-encapsulated devices, which were fabricated by a dry-transfer approach (Methods), a small graphene flake was encapsulated between two thick layers of h-BN, providing isolation from an underlying SiO$_2$ substrate. The carrier concentration in these devices was controlled by means of a top gate (see Figure 2), whose dielectric was formed by the upper h-BN layer.

The essential principle of our pulsed measurements is illustrated in Figure 2. This shows how a short voltage pulse (of amplitude V_p, duration T, and rise time t_r) is applied repetitively (at a frequency f_r) to the source line ("In", Figure 2) of a microwave graphene FET. The signal is sourced via an on-chip coplanar waveguide designed to provide 50 Ω matching to the graphene.[17] A 50 Ω ruthenium oxide resistor ensures a matched termination on the input line (see Figure 2), and the resulting transient current that flows to the drain is measured by feeding this line ("Out", Figure 2) into the 50 Ω input of a real-time oscilloscope. The pulse duration used in our experiments was varied from 25 ns to 100 μs, while the repetition frequency could be set in the range of 10 kHz−1 MHz. Through variation of these parameters, we were able to distinguish and fully investigate the role of self-heating and hot-carrier trapping in the devices.

We start by assessing the differences in behavior exhibited by the graphene/h-BN and graphene-on-SiO$_2$ devices under linear operation. Here, a small dc voltage (∼mV) is applied to generate a drain current, the variation of which is measured while sweeping the gate voltage that controls the carrier concentration in the channel. In Figure 3, we show that, for the graphene-on-SiO$_2$ device, such an experiment generates significant hysteresis when sweeping the gate voltage in opposite directions. This behavior is well known for devices formed on SiO$_2$, in which it is typically attributed to the charging of interfacial states and of deep traps in the oxide layer.[21,23,29−33] In marked contrast, the corresponding measurement for a graphene-encapsulated device shows no measurable hysteresis, suggesting that both of these charging mechanisms are suppressed when h-BN is used as the graphene substrate. It should be noted here that, in spite of the very different sweep ranges employed in these measurements, the corresponding variations of carrier concentration are quite similar for the two devices. For the BN-encapsulated device, variation of the top-gate voltage from −20 to 0 V corresponds to a respective change from 2.0×10^{12} holes cm^{-2} to 1.2×10^{12} electrons cm^{-2}. Similarly, for the graphene-on-SiO$_2$ FET, the back-gate voltage range (of 0 to 60 V) implies a change from 2.9×10^{12} holes cm^{-2} to 1.4×10^{12} electrons
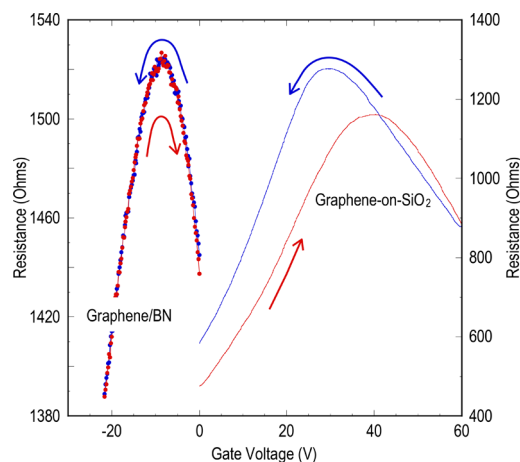

Figure 3. Comparison of hysteresis in the transfer curves of graphene-on-SiO$_2$ (right vertical scale) and h-BN-encapsulated (monolayer graphene, left vertical scale) FETs. The gate voltage sweep direction is indicated by the arrows in the figure, and the measurements were performed by applying a dc drain bias of 25 mV to both devices. For the graphene/h-BN heterostructure, filled symbols are plotted to indicate the extent to which the transfer curve shows no measurable hysteresis. Gate voltage sweep rates were 200 and 100 mV/s for the h-BN-encapsulated and graphene-on-SiO$_2$ devices, respectively.

cm^{-2}. In both of the devices, the maximum range of the gate voltage sweep was limited by the need to minimize gate-current leakage. It is also noted that the relative change of resistance is smaller for the BN-encapsulated device; this most likely reflects the influence of contact resistance in the two-probe geometry that is required[17] for our pulsed measurements (the graphene-on-SiO$_2$ device, on the other hand, was measured in a four-probe configuration).

While the results of Figure 3 point to the absence of charging effects in h-BN-encapsulated graphene FETs, it is important to stress that these results were obtained for small-signal operation (average drain fields ∼V/cm). Consequently, they do not address the question of whether such effects can be expected to appear when these devices are operated under the hot-carrier conditions that are more pertinent to practical device operation. For an answer to this question, we study how the pulsed current−voltage characteristics of the devices vary as a function of pulse duration. In the inset to Figure 4, we show the results of such an experiment for a graphene-on-SiO$_2$ device (to allow a comparison with the data in the main panel, the pulse amplitude is converted into a corresponding electric field in this figure). As the pulse duration is increased, the steady-state current (measured at the end of the pulse) exhibits an apparent region of negative differential conductance, which begins at progressively lower fields as the pulse length is increased. This is not some intrinsic feature of hot-carrier transport in graphene but, as noted previously in ref 17, rather results from the onset of charge trapping under high drain fields (>10 kV/cm).

In contrast to the behavior in the inset, in the main panel of Figure 4, we show corresponding measurements of the pulsed current−voltage characteristics of a h-BN-encapsulated (monolayer) graphene device. It is clear that these data are independent of pulse duration, even when the pulse length is increased to as much as a microsecond, in spite of the fact that the corresponding field in the channel reaches values as large as those shown in the inset.
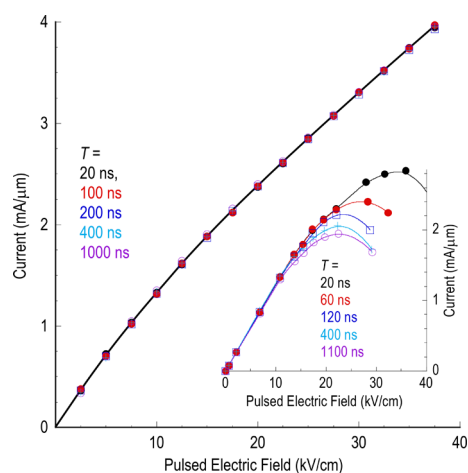
Figure 4. The main panel plots the results of pulsed current−voltage measurements of the h-BN-encapsulated monolayer graphene FET. Results are plotted for various pulse durations (indicated), and the solid line is a guide to the eye. The top-gate voltage in these measurements was −3 V, close to the Dirac point of the device. Inset: corresponding measurements for a (bilayer) graphene-on-SiO$_2$ device. The inset is adapted with permission from Ramamoorthy, H.; Somphonsane, R.; Radice, J.; He, G.; Kwan, C.-P.; Bird, J. P. "Freeing" graphene from its substrate: observing intrinsic velocity saturation with rapid electrical pulsing. *Nano. Lett.* **2016**, *16*, 399−403. Copyright 2015 American Chemical Society.

For a more comprehensive analysis of the influence of self-heating and hot-carrier trapping in the encapsulated devices, it is helpful to use the transient current to define a pulse-dependent resistance. This is done by dividing the value of the applied voltage (V_p) by the peak value that the current reaches during the on-stage of the pulse. In Figure 5, we plot the gate-voltage-dependent variation of this resistance for a number of different pulse amplitudes. It is apparent from this figure that the increase of the pulse amplitude influences this resistance differently in the monolayer (Figure 5b) and bilayer (Figure 5a) devices; in the former case, the increase of V_p causes the transient resistance to increase, while in the latter it gives rise to a decrease of resistance. These differences have actually been noted previously in temperature-dependent studies of the linear (dc) conductance of monolayer and bilayer graphene[34−39] and have been explained in terms of the very different way in which electron−phonon scattering is screened in these materials.[38,39] Particularly beneficial here is the behavior observed in the bilayer device (Figure 5a) in which larger pulsed voltage (i.e., stronger heating) results in a decrease of the overall resistance level. This should be in contrast to the effects of charge trapping, which can be expected to result in a decrease of current or an increase of resistance. In the discussion that follows, we exploit these opposite characteristics to distinguish the influence of heating and trapping on the transient behavior.

Returning to the data of Figure 4, the absence of any dependence on pulse duration in the main panel not only indicates an absence of trapping but also demonstrates that self-heating is negligible in these measurements. This can be attributed to the low repetition frequency (f_r = 100 kHz) used in these measurements, the choice of which ensures that successive pulses remain well isolated from one another and that there is no "build up" of heat in the dielectric layers.[18] In order to study self-heating effects, we therefore increase the
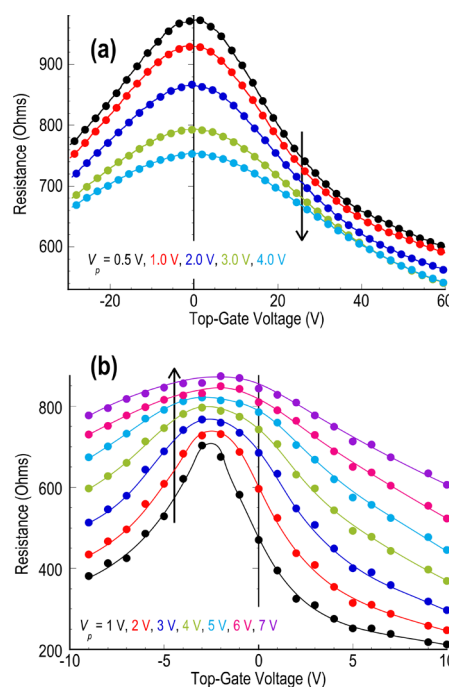

Figure 5. (a) Variation of resistance as a function of gate voltage determined for the h-BN-encapsulated bilayer graphene FET at the indicated pulsed-voltage amplitudes. Pulse duration, T = 20 ns; repetition frequency f_r = 10 kHz. (b) Variation of resistance as a function of gate voltage determined for the h-BN-encapsulated monolayer graphene FET at the indicated pulsed-voltage amplitudes. Pulse duration, T = 60 ns; repetition frequency f_r = 10 kHz. Arrows indicate the tendency exhibited by the resistance as the pulse amplitude (V_p) is increased.

repetition frequency (to 1 MHz) and vary the pulse duration over a range of 40−750 ns, which allows us to study the evolution from isolated pulses to near-dc biasing. The results of such an experiment are presented in Figure 6a,b, of which the applied pulse amplitude (0.5 V) corresponds to an average channel field of 10 kV/cm. Figure 6a represents the transient behavior observed near the charge-neutrality point, while in Figure 6b the gate voltage implies a corresponding hole doping of 5.8 × 10^{12} cm$^{−2}$. Regardless of these differences, the two figures reveal essentially the same behavior, namely, a systematic increase in the overall current level as pulse duration is increased. (Note that V_{out} is the voltage detected at the 50 Ω input to the oscilloscope and thus is directly proportional to the transient current). This increase is the effect of self-heating, which leads to a decrease in the resistance of bilayer graphene with increased temperature, as observed already in Figure 5a.

In Figure 6c,d, the amplitude of the voltage pulses is increased to 3.0 V, corresponding to an average electric field of 60 kV/cm. The resulting behavior differs very strongly between the two panels, with Figure 6c exhibiting the self-heating behavior noted already for Figure 6a,b. In Figure 6d, however, the transient variations are more complicated. For given pulse duration, the transient current grows over time, reminiscent of the heating signatures present in Figure 6a−c. As the pulse duration is increased, however, there is a systematic decrease in the overall current level, behavior that is indicative of carrier trapping.

The interplay of self-heating and trapping is further demonstrated in Figure 7 in which the repetition frequency
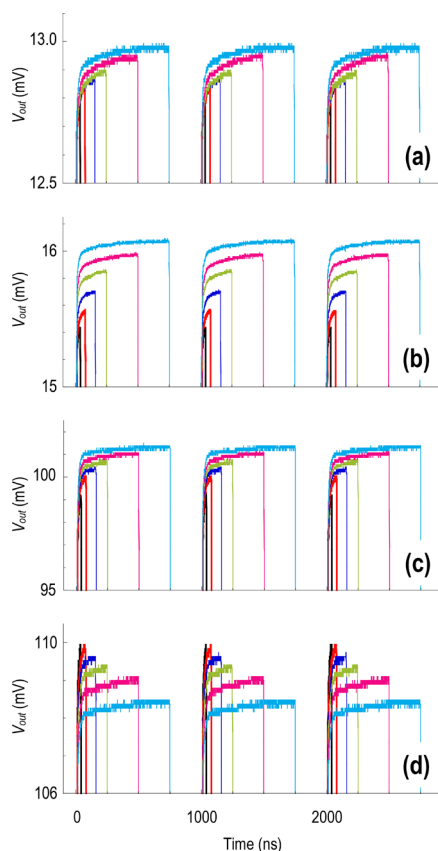
Figure 6. Pulsed measurements of the h-BN-encapsulated bilayer device at a repetition frequency of 1 MHz. Pulse duration is varied from 40−750 ns in each of the panels. To highlight the time-dependent variations exhibited by these data, the various panels focus on the range of data near the top of the voltage pulse. (a) Top-gate voltage = 0 V, V_p = 0.5 V. (b) Top-gate voltage = −40 V, V_p = 0.5 V. (c) Top-gate voltage = 0 V, V_p = 3.0 V. (d) Top-gate voltage = −40 V, V_p = 3.0 V. The average field in the channel is 10 kV/cm (60 kV/cm) in panels (a) and (b) [panels (c) and (d)].
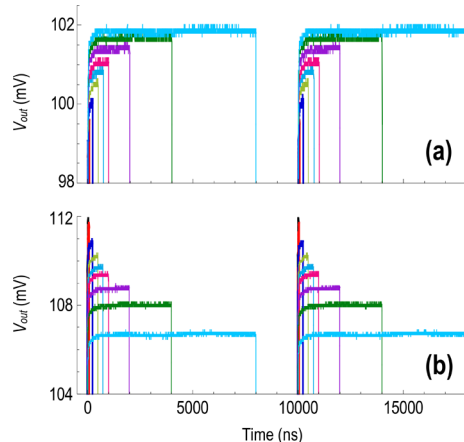

Figure 7. Pulsed measurements of the h-BN-encapsulated bilayer device at a repetition frequency of 100 kHz. Pulse duration is varied from 40−8000 ns in the two panels. To highlight the time-dependent variations exhibited by these data, each panel focuses on the range of data near the top of the voltage pulse. (a) Top-gate voltage = 0 V, V_p = 3.0 V. (b) Top-gate voltage = −40 V, V_p = 3.0 V. The average field in the channel is 60 kV/cm in panels (a) and (b).

has been reduced to 100 kHz, allowing us to apply even longer pulses. In Figure 7a, the behavior is much like that in Figure 6c, with the data showing only the signatures of heating (current increasing with pulse duration). The data of Figure 7b, on the other hand, are clearly dominated by carrier trapping, with the overall current level systematically decreasing as the pulse length is increased.

The key conclusion of Figures 6 and 7 is that trapping effects may dominate the transient response of the graphene/h-BN system but only when the drain and gate fields are both large; for an applied gate voltage of −40 V, the corresponding gate field is 26 MV/cm, which can be expected to induce significant band bending in the upper h-BN. It is this bending that presumably facilitates the injection of hot carriers from the graphene layer, when the field in that layer is also large.

Turning to the issue of self-heating, this should be governed by a characteristic time constant (τ), whose value is related to the thermal resistances and capacitances in the problem (see Figure 1a). The value of this parameter may be inferred experimentally by fitting the form of the transient current variation, observed under conditions where trapping is insignificant. Some examples of this are provided in Figure 8,
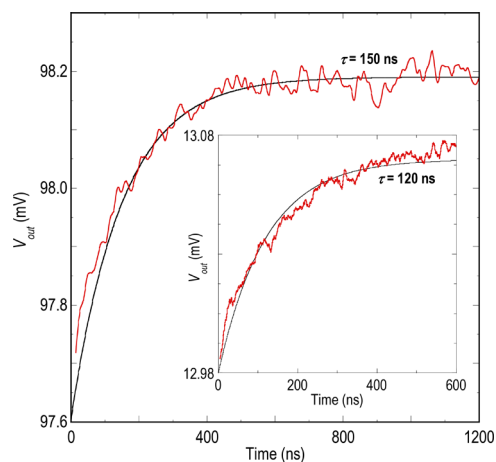

Figure 8. Estimation of the thermal time constant from the transient current. Measurements of the h-BN-encapsulated bilayer device at a pulse repetition frequency f_r = 100 kHz. The top gate was grounded in these measurements, and the pulse amplitudes were 3.0 and 0.5 V in the main panel and the inset, respectively. Solid lines are fits through the data to the form of eq 1.

the data of which were obtained for the bilayer device with the top gate grounded (i.e., V_g = 0 V). The data of the main panel were obtained for a pulse amplitude V_p of 3.0 V, while for those in the inset V_p was 0.5 V. In both of these figures, we fit the transient current variation observed at the top of the pulse to the time-dependent form

$$V_{out}(t) = V_0 + \Delta V(1 - e^{-t/\tau}) \tag{1}$$

where V_0 is the voltage initially attained at the end of the rising edge of the pulse (defined here as $t = 0$) and ΔV and τ are treated as fit parameters. For the data shown in the inset to Figure 8, we obtain a τ of 120 ns, while for that in the main panel we find a τ of 150 ns; these two estimates are considered to be consistent with one another.

Finally, we compare the results of our pulsed measurements of these devices with those obtained under conditions of dc biasing. Representative results are plotted in Figure 9, panels
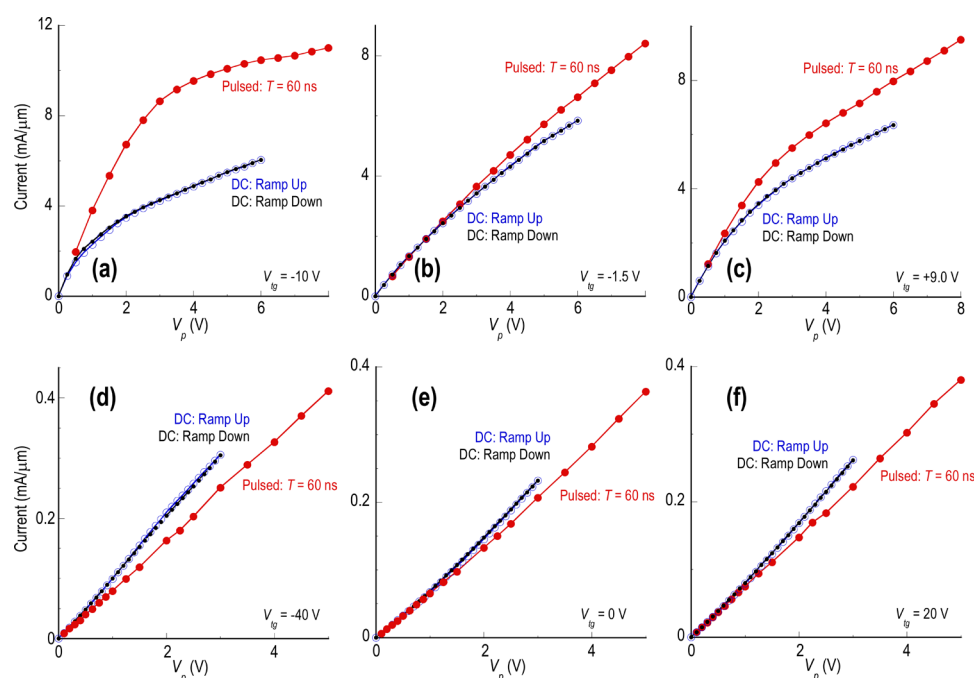
Figure 9. Comparison of transient and dc current−voltage characteristics for (a−c) h-BN-encapsulated monolayer device and (d−f) h-BN-encapsulated bilayer device. The various panels correspond to different values of the top-gate voltage (V_{tg}, indicated). Panels (b) and (e) are at the Dirac point of the devices, while panels (a) and (d) [(c) and (f)] represent examples of heavy hole (electron) doping. The pulse repetition frequency in these measurements f_r was 100 kHz, while the pulse period T was 60 ns.

(a−c) of which were obtained for the monolayer device and panels (d−f) were obtained for the bilayer one. Results are shown for different gate voltages, with panels (b) and (e) demonstrating the behavior obtained near the respective Dirac points (compared with Figure 5). Panels (a) and (d), on the other hand, correspond to hole doping of the FET channels, while panels (c) and (f) were obtained for electron doping. Beginning with the monolayer device, we see that, in all three panels, the data obtained by rapid pulsing attain higher current levels than the corresponding dc data. The difference between pulsed and dc measurements is smallest at the Dirac point (Figure 9b) and more pronounced for strong hole doping (Figure 9a). For the bilayer device, however, we obtain the opposite result, with the current being systematically smaller in the pulsed experiments. These different observations can be explained in terms of increased self-heating under dc biasing, if we recall that the temperature coefficient of the resistance is of opposite sign for monolayer and bilayer graphene.[34−39] (Physically, the reason for this is the very different way in which electron−phonon scattering is screened in these materials.[38,39]) In the monolayer FET, increased self-heating should lead to increased resistance and thus to a decrease of the current. This is precisely what is seen in the experiment (Figure 9a−c in which the current observed for dc conditions is systematically lower than that obtained under transient pulsing. Similarly, for bilayer graphene, self-heating should lower the channel resistance, increasing the overall current level, precisely what is seen in the results of Figure 9d−f. A comparison of the monolayer and bilayer data reveals that the difference between dc and pulsed biasing is strongest for the monolayer device. This is consistent with the behavior shown in Figure 5 in which the monolayer FET exhibits a larger relative resistance change as gate voltage is varied than the bilayer one.

■ DISCUSSION

The objective of this work was to evaluate the influence of self-heating and hot-carrier trapping on the operation of h-BN-encapsulated graphene transistors and to compare these behaviors with those exhibited by more common, graphene-on-SiO_2, devices. With regard to the role of carrier trapping, the improved immunity offered by h-BN encapsulation was suggested by the results of measurements of the small-signal transconductance of the different devices (Figure 3). These revealed a complete suppression of the hysteresis that typically plagues graphene-on-SiO_2 devices, behavior that has been attributed to charging of interfacial and deep oxide traps.[21,23,29−32] More importantly, however, through our transient studies of nonequilibrium operation, we were able to confirm that the immunity offered by h-BN encapsulation persists even in the hot-carrier limit, pertinent to the operation of practical devices. This was demonstrated most clearly in Figure 4, where the maximum current measured during transient pulsing was shown to be independent of the pulse duration. Through further studies, we were able to establish that signatures of trapping can be observed in the encapsulated system but that this requires the simultaneous presence of large gate and drain fields (see Figures 6d and 7b). From studies in which it is incorporated as the tunnel barrier in vertical-transport devices, h-BN has been shown to possess various native defects that can mediate current under the application of large electric fields.[40−43] While these defects are not expected to be present at the concentrations found in SiO_2, one possibility is that they may mediate the trapping of hot carriers in h-BN via the Poole−Frenkel mechanism.[44] This phenomenon is well-known from the study of conduction mechanisms in dielectrics and refers to the ability of a strong electric field to lower the potential barrier associated with impurity sites, thereby allowing them to mediate the capture and/or emission

of energetic carriers. To definitively assert the role of the Poole−Frenkel mechanism in our experiments, it would be necessary to demonstrate that the leakage current exhibited by the gate follows the characteristic dependence on the electric field associated with this effect.[44] Since the gate leakage remained at subnanoampere levels in our experiments, however, it was not possible to make this identification. Nonetheless, in our experiments, we note that the signatures of trapping are observed once the gate and (average) drain fields reach values of orders 10^7 and 10^5 V/cm, respectively. We suggest that this very large gate field lowers the energy barrier associated with the h-BN trapping sites, allowing the high drain field to inject hot carriers into these sites from the graphene. Nonetheless, in spite of this behavior, the essential message that should be taken away from this study is that h-BN encapsulation offers an effective means to significantly suppress (if not completely eliminate) the influence of hot-carrier trapping in graphene devices.

Turning next to the issue of self-heating, our study provides valuable insight into how this influences device operation. This is essentially achieved by using the transient conductance of the graphene to "detect" phonon excitation in the surrounding dielectric layers of the device. The sequence of events that is initiated when the pulsed voltage is first applied to the device begins with the thermalization of graphene's carriers at an effective hot temperature, following which these nonequilibrium carriers lose energy to the external reservoirs and to the phonon modes of the graphene itself. Essentially, these processes may be viewed as instantaneous, at least on the timescale of our measurements.[17] Ultimately, however, phonon conduction will transfer heat from the graphene to the surrounding dielectrics, generating nonequilibrium phonon populations in these layers. This results in a "feedback" process in which carriers in the graphene layer can now be additionally scattered through their interaction with nonequilibrium phonons in the h-BN layers, generating an associated change in the transistor current. It is this time-dependent growth of phonon-induced scattering that we are essentially watching when (in the absence of charging) we observe time-dependent variations of the transient current in our experiments (see Figures 6a−c and 8). To support this argument, it is helpful to estimate the various thermal time constants associated with the different layers indicated in Figure 1a. While we refer the reader to the Methods for the details of this analysis, by accounting for heat conduction through the constituent dielectric layers, we estimate a total time constant of ∼130 ns. This value is in excellent agreement with that determined experimentally (100−150 ns, see Figure 8) for the self-heating, confirming our understanding of this behavior.

In conclusion, in this research article, we have used transient measurements to investigate the details of self-heating and charge trapping in h-BN-encapsulated graphene transistors operated under strongly nonequilibrium conditions. Relative to more standard devices fabricated on SiO_2 substrates, encapsulation has been shown to lead to an enhanced immunity to charge trapping, the influence of which is only apparent under the combined influence of strong gate and drain electric fields. The strong gate field can be expected to lower the barriers associated with native defects in the h-BN, allowing energetic carriers to then be captured from the channel in a Poole−Frenkel type process. Self-heating in these devices was identified through the observation of time-dependent variations of the current in graphene and was

found to be described by a time constant consistent with expectations for nonequilibrium phonon conduction into the dielectric layers of the device. The importance of proper substrate selection for the performance of graphene FETs has long been appreciated theoretically.[45−48] Our results here confirm that h-BN-encapsulated graphene devices provide an excellent system for implementations in which operation under strongly nonequilibrium conditions is desired. It will be interesting to extend these measurements in the future to graphene encapsulated in other 2D materials,[1] including various transition-metal dichalcogenides (MoS_2, WS_2, WSe_2, etc.).

■ METHODS

Device Fabrication. Two types of graphene transistors were fabricated for this study, those encapsulated in h-BN and more standard graphene-on-SiO_2 devices. While the fabrication of the latter devices has been described in detail previously,[19,20] the encapsulated devices were realized through a modified dry-transfer process. In this approach, Ti/Au source and drain electrodes were first fabricated on a flake of h-BN, exfoliated onto a (300 nm thick) SiO_2 layer. (The SiO_2 was formed on top of a resistive Si substrate, whose metallized bottom surface was used to define a ground plane for the pulsed measurements.[19]) Next, small graphene flakes, exfoliated onto another SiO_2/Si substrate, were picked up using a h-BN flake that had previously been attached to a polypropylene carbonate (PPC) film. Using a transfer stage, the graphene/h-BN heterostructure was then pressed against the aforementioned electrodes, following which the PPC film was removed by application of mild heat (90 °C) and subsequent solubilization in chloroform. Following this, the device was annealed in a reducing atmosphere for 1 h at 523 K to improve the quality of the electrical contacts. This completed the encapsulation process, following which electron beam lithography and metal lift-off were used to realize 50 Ω matched on-chip coplanar waveguides for the pulsed measurements.[19] Two different encapsulated devices were studied here, one consisting of monolayer graphene and the other being a bilayer device. The source−drain separations in these devices were 1 and 0.5 μm, respectively. In the monolayer system, the thicknesses of the upper and lower layers (as determined by atomic force microscopy) were 152 ± 4 and 161 ± 5 μm, respectively. Corresponding figures for the bilayer device were 152 ± 4 and 152 ± 3 μm.

Transient Measurements. Pulsed current−voltage characteristics of the devices were measured at room temperature in a repetitive-pulsing scheme that has been described in detail in refs 17 and 18. The measurements were made in a custom-designed setup with full (50 Ω) impedance matching. The device chip was mounted on an FR-4 laminate board, allowing the signal lines of its coplanar waveguide to be connected to semirigid coaxial cables (see Figure 2). Repetitive pulses were applied with an AVTECH generator, providing a maximum pulse amplitude of 10 V and a repetition frequency that could be varied from 10 kHz−1 MHz. Resulting output pulses were then captured by a fast oscilloscope (either a Tektronix CSA8000B digital-sampling oscilloscope with 50 GHz bandwidth or a Keysight MSOX6004A mixed-signal oscilloscope with 6 GHz bandwidth).

Estimation of Thermal Time Constants. Thermal time constants ($\tau = \mathcal{R}C$) were estimated for the different layers of the device using their known thermal properties and their

physical dimensions. The latter was determined from inspection using a combination of atomic force and optical microscopy. Assumed thermal conductivities were 25, 1.3, and 80 W/(m·K) for h-BN, SiO_2, and Si, respectively, while corresponding specific heats were taken to be 700, 680, and 750 J/(kg·K). Using these values, we arrived at estimates for the corresponding thermal time constants $\tau_{\text{h-BN}}$, τ_{SiO_2}, and τ_{Si} of ~1.5, ~118, and ~6 ns, from which the total time constant τ was estimated as ~130 ns.

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Notes

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