Memory characteristics of InAs quantum dots embedded in GaAs quantum well

E. S. Kannan,[1] Gil-Ho Kim,[1,a)] and D. A. Ritchie[2]
[1]*Department of Electronic and Electrical Engineering and Sungkyunkwan University Advanced Institute of Nanotechnology, Sungkyunkwan University, Suwon 440-746, Republic of Korea*
[2]*Cavendish Laboratory, Madingley Road, J.J. Thomson Avenue, Cambridge CB3 0HE, United Kingdom*

(Received 20 March 2009; accepted 10 September 2009; published online 9 October 2009)

The memory characteristics of InAs based quantum dot (QD) memory devices has been investigated by carrying out capacitance-voltage and current-voltage measurements. The dots which were embedded in the GaAs quantum well were charged by the electrons from the two dimensional electron gas and a clockwise hysteresis loop is observed on cyclically sweeping the gate bias. The number of trapped electrons is found to be two orders of magnitude lesser than the QD density. Interdot Coulombic interactions and phonon assisted electron tunneling was found to significantly affect the charge trapping ability of the QDs. © *2009 American Institute of Physics*.
[doi:10.1063/1.3242347]

Today's commercial market is mainly dominated by dynamic random access memory and flash memories.[1] These devices which are primarily silicon based are limited by small number of material combinations and a limited number of fixed band offsets. In this scenario, the quantum dot (QD) memory devices based on III-V compound semiconductors apart from offering many possible material compositions provide better quality of crystalline heterostructure and band structure engineering. Moreover the read/write process in QD devices require low operation voltages since tunneling is employed for carrier injection and depletion.[2] Already these devices were found to possess higher read/write speeds, more storage capacity, greater endurance, and are more reliable in comparison to other nonvolatile memory devices.[3,4] Notwithstanding all these unique advantages, the QD memories are still confined only to low temperature regime due to the relatively small energy barriers for thermal excitation and loss of carriers to the wetting layer or continuum.[5]

To ensure reliable operation of QD devices, the electrons have to be stored preferentially in the intrinsic energy level of the dots. One way of achieving this is by embedding QDs in the quantum well which enhances the coupling between the electrons in the two-dimensional electron gas (2DEG) and the QDs.[6] The memory device based on this structure consume very less power and will be much faster due to less tunneling time.[2] However the absence of tunneling barrier makes the charge retention in the embedded QDs a very challenging issue. In this present study, we investigated the trapping, detrapping and charge retention capabilities of InAs QDs embedded in GaAs quantum well by carrying out capacitance-voltage (*C-V*) and current-voltage (*I-V*) measurement at different temperatures and frequencies.

The sample used for this study is a GaAs/AlGaAs single quantum well structure grown by molecular beam epitaxy. The heterostructure was grown on GaAs substrate and consists of an 18 nm wide $GaAs/Al_{0.33}Ga_{0.67}As$ quantum well that was modulation doped using a 40 nm spacer layer and the density of 2DEG at zero bias is found to be 2.95×10^{11} cm^{-2}. InAs QDs were then inserted at the center of the quantum well.[7,8] Ohmic contacts to the QDs and the surface Schottky gates were fabricated using standard photolithographic technique. The QD density determined from the plain view transmission electron microscopic image was found to be 5.8×10^9 cm^{-2}.[9] From the high resolution TEM image, the height and width of the dots were found to be 8 and 36 nm respectively.[7,9] The sample was then loaded into a closed cycle cryostat to perform the *I-V* and *C-V* measurements. *C-V* measurements were taken by connecting the sensing terminal to the ohmic and the signal $[ac(20\ mV_{rms})+dc]$ terminal to the gate. For the *I-V* measurements three terminal configuration was employed. A constant d.c bias of 0.1 V was applied between the source-drain contacts and the variation in drain current was recorded as a function of gate voltage. The sweeping rate for the gate voltage was maintained at 5 mV/sec for the *I-V* and *C-V* measurements.

Figure 1 shows the *C-V* and *I-V* characteristics of the QD sample. The clockwise hysteresis loop observed in the *C-V* and *I-V* traces on ramping the gate bias (V_g) cyclically is a clear signature of electrons being trapped in the QDs.[4] The lower drain current observed during the reverse sweep confirms the decrease in the 2DEG density. To study the gate voltage dependence, the hysteresis characteristics in the con-

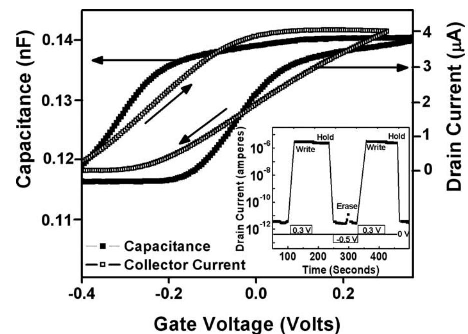

FIG. 1. Capacitance-voltage and current-voltage characteristics of the QD sample at 100 K. Inset: Real time measurement of collector current on applying write/erase pulse through the gate. Source-drain bias for the *I-V* measurement is fixed at 100 mV.

a)Author to whom correspondence should be addressed. Electronic mail: ghkim@skku.edu.

 © 2009 American Institute of Physics

Downloaded 11 Oct 2009 to 115.145.155.112. Redistribution subject to AIP license or copyright; see http://apl.aip.org/apl/copyright.jsp

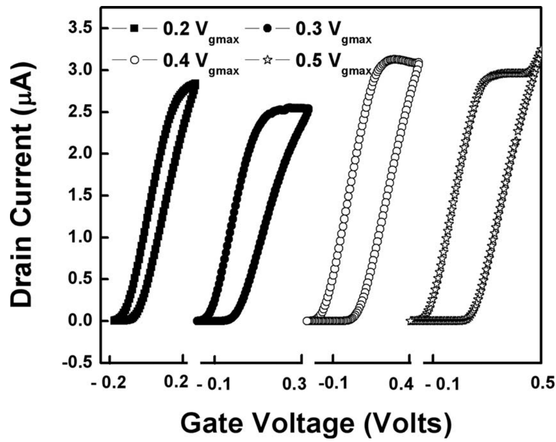

FIG. 2. Clockwise hysteresis loop observed in the conductance trace for V_{gmax}=0.2, 0.3, 0.4, and 0.5 V at 100 K. The source drain bias is fixed at 100 mV.

ductance trace was carried out by changing the maximum gate voltage (V_{gmax}) to which the sweep was returned. For different V_{gmax} the corresponding change in the hysteresis behavior is studied. No hysteresis was observed when the sweeping voltage was limited to $V_{gmax}=0.1$ V. Hysteresis was observed on increasing V_{gmax} above this threshold limit. This indicates that the charge trapping in the QDs occurs only when the gate voltage was increased above 0.1 V. The study is then carried out for V_{gmax}=0.2, 0.3, 0.4, and 0.5 V and the results are shown in Fig. 2. On incrementing the range of V_{gmax}, the area of the hysteresis loop increased proportionally (Fig. 2). Since the area enclosed by the hysteresis loop is directly related to the number of electrons trapped by the QDs, more number of electrons will be lost from the 2DEG with increase in V_{gmax}. As a result the negative threshold voltage required to completely deplete the 2DEG shifted toward 0 V as V_{gmax} is increased.

The capacitance response from the heterostructures with embedded QDs will be a combination of the capacitance of the QDs (C_{QD}) in series with the resistance of the 2DEG (R). The RC time constant of the equivalent circuit is given by $\tau = C_{QD}R$. Using the capacitance and resistance data from Fig. 1 the maximum value of τ is found to be 14 ms, which corresponds to a frequency of 10 kHz (approximately). As the frequency of the ac signal is increased from 10 to 100 kHz, the area of hysteresis is reduced (Fig. 3). At 200 kHz the hysteresis is completely absent due to the inability of the electrons to synchronize with the ac signal at a higher frequency. The frequency dependent measurements are carried out at 10 K to suppress the thermal excitation of electrons from the InAs dots to the 2DEG.

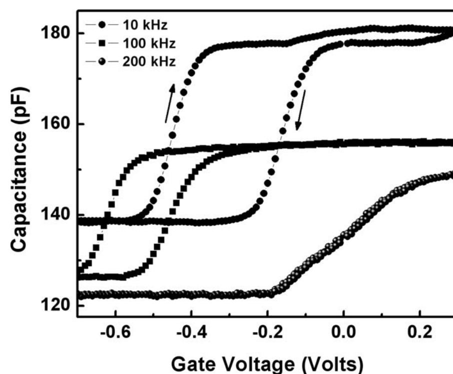

FIG. 3. *C-V* characteristics of the sample at three different frequencies. The measurement temperature is 10 K.

The change in the capacitance with respect to the gate can be explained based upon the change in the depletion layer width caused by the depletion of carriers in the 2DEG. In the region between $V_g = -0.5$ and -0.4 V during the forward sweep (from negative to positive V_g), the 2DEG and the QDs are in a state of depletion. The width of the depletion region will extend beyond the quantum well region and the capacitance in this regime will be smaller. As V_g is increased, the electrons will gradually populate the quantum well and the width of the depletion layer decreases. The 2DEG density will also increase rapidly and a sharp linear increase in capacitance is observed between $V_g = -0.4$ and 0.1 V. Beyond $V_g = 0.1$ V, the electrons from the 2DEG tunnel into the QDs due to the decrease in the height of the tunneling barrier. During the process of electron trapping in the QDs, the capacitance remains constant. The invariance of the capacitance with V_g in the charging regime (from 0.1 to $0.4V_g$) arises due to two important factors.

(1) The increase in 2DEG density with V_g will be compensated by the electrons tunneling into the QDs. Therefore the width of the depletion region will remain almost constant.
(2) Second when the QDs trap the electrons they acquire negative charge. As V_g increases, more and more electrons will be trapped in the QDs. The negative potential of the dots will proportionally increase and screen the electric field from the gate. As a result of this screening effect, the rate of change of capacitance with the gate voltage will be very less.

A smaller capacitance is observed during the reverse sweep due to the larger depletion width as some of the electrons remain trapped in the QDs. For $V_g < -0.1$ V, the electrons which tunneled into the QDs from the 2DEG will start to deplete. At -0.5 V almost all the electrons from the QDs are removed and the forward and reverse capacitance trace will intersect each other at this point. The device is now completely reset and ready for the next cycle of operation. The voltage sweep is then repeated several times and similar hysteresis trace is reproduced without any sign of deterioration.

From the hysteresis curve, the number of electrons that are trapped in the QDs can be calculated from the increment in the depletion layer width at $V_g = 0$ V which inturn can be identified from the difference in the capacitance values. The number of electrons trapped in the QDs can be determined from the formula

$$n_{QD} = (C_F - C_R) \times \Delta V / eA, \quad (1)$$

where n_{QD} is the number of electrons in the QD, $C_{F,R}$ is the value of capacitance at the zero bias during the forward and reverse sweeps, e is the electronic charge, A is the area of the sample, and ΔV is the hysteresis width. From the *C-V* characteristics of Fig. 1, the number of trapped electrons to be approximately 1.27×10^7 electrons/cm^2. The densities of the dots being in the order of 10^9 cm^{-2}, it is clear that, not all the dots contain electrons. A simple physical argument can be put forth to explain this observation. The charge storing ability of the QD ensemble depends strongly on two

Downloaded 11 Oct 2009 to 115.145.155.112. Redistribution subject to AIP license or copyright; see http://apl.aip.org/apl/copyright.jsp

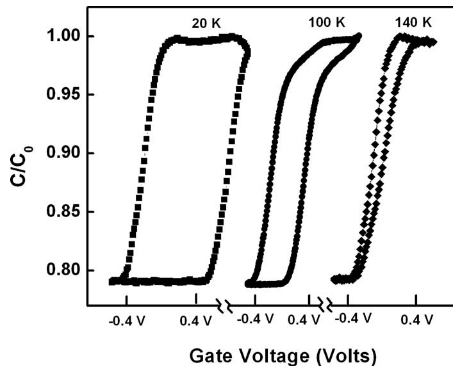

FIG. 4. Temperature dependent hysteresis characteristics observed in the capacitance measurement.

parameters; one is the Coulombic interaction and the other is the tunneling of electrons between the dots and the 2DEG. During the writing operation (forward sweep), when the charges begin to accumulate in the QDs, the Coulombic interaction between the dots increases significantly. Since the electron distribution in the QD layer will be random, the dots which trap electrons first exert Coulombic repulsive force on the electrons entering into the neighboring dots. This reduces the charge trapping probability of the nearby dots.[10] At any finite temperature, the interaction between electrons and phonons will further decrease the electron trapping ability of the QDs. On decreasing the temperature, this phonon assisted tunneling can be suppressed and the area of hysteresis increases (Fig. 4). The number of trapped electrons increases from 3.37×10^6 to 1.35×10^8 electrons/cm^2 when the temperature is decreased from 140 to 20 K.

The charge retention time was studied by carrying out the real time measurement of the collector current as the gate bias is switched between −0.5 and 0.3 V (erase/write pulse). The electrons were first discharged from the QDs by applying a negative pulse of −0.5 V. A write voltage pulse of 0.3 V is then applied for few seconds and the change in the collector current was monitored as a function of time under the zero bias condition. As shown in the inset of Fig. 1, the collector current in the device remained stable at 1.9 μA, which is the value of the current observed at $V_g=0$ (Fig. 1) after the QDs are saturated with electrons. During the hold period the collector current did not increase, which is an indication that the electrons are not discharged from the QDs. A charge retention time of several seconds can be determined from the hold period. This is in agreement with the theoretically predicted value for the memory devices based on InAs QDs.[11]

In conclusion, we have investigated the charge trapping ability of the QD memory devices with different dot density. Clockwise hysteresis loop is observed in the *C-V* and *I-V* measurements due to the electrons being trapped in the QDs. The trapping density calculated from the hysteresis curve revealed that the number of stored electrons is considerably less than the density of the dots. Interdot Coulombic interaction and phonon assisted tunneling was found to significantly affect the trapping density in the QDs. The most important advantage of our device is that the entire memory operation can be carried out by applying a voltage of the order of few hundred millivolts. Since the device consumes less power, it holds great potential toward fabricating low power electrically driven memory devices.

This research was supported by World Class Univeristy (WCU) program through the National Research Foundation of Korea (NRF) funded by the Ministry of Education, Science and Technology (Grant No. R32-2008-000-10204-0).

[1]R. Waser, *Microelectronics and Information Technology* (Wiley-VCH, Berlin, 2003).
[2]S. L. Chuang and N. Holonyak, Jr., Appl. Phys. Lett. **80**, 1270 (2002).
[3]A. Marent, M. Geller, A. Schliwa, D. Feise, K. Pötschke, D. Bimberg, N. Akçay, and N. Öncan, Appl. Phys. Lett. **91**, 242109 (2007).
[4]M. Geller, A. Marent, T. Nowozin, D. Bimberg, N. Akçay, and N. Öncan, Appl. Phys. Lett. **92**, 092108 (2008).
[5]M. S. Skolnick and D. J. Mowbray, Annu. Rev. Mater. Res. **34**, 181 (2004).
[6]E. S. Kannan, G. H. Kim, I. Farrer, and D. A. Ritchie, Phys. Status Solidi C **6**, 813 (2009).
[7]Gil-Ho Kim, D.A. Ritchie, C.-T. Liang, G. D. Lian, J. Yuan, M. Pepper, and L. M. Brown, Appl. Phys. Lett. **78**, 3896 (2001).
[8]G. H. Kim, D. A. Ritchie, M. Pepper, G. D. Lian, J. Yuan, and L. M. Brown, Appl. Phys. Lett. **73**, 2468 (1998).
[9]G. D. Lian, J. Yuan, L. M. Brown, G. H. Kim, and D. A. Ritchie, Appl. Phys. Lett. **73**, 49 (1998).
[10]M. Prada and P. Harrison, New J. Phys. **6**, 30 (2004).
[11]G. Iannaccone and P. Coli, Appl. Phys. Lett. **78**, 2046 (2001).

Downloaded 11 Oct 2009 to 115.145.155.112. Redistribution subject to AIP license or copyright; see http://apl.aip.org/apl/copyright.jsp