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Charge trapping in quantum dot memory devices with different dot densities

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Abstract
The memory characteristics of electrically driven quantum dot (QD) memory devices with different dot densities were investigated by capacitance–voltage (C–V) and current–voltage (I–V) measurements at 100 K. The dots which were embedded in the GaAs quantum well were charged by the electrons from the two-dimensional electron gas at positive gate bias. On cyclically sweeping the gate bias, a clockwise hysteresis loop is observed in the capacitance and conductance trace. The number of trapped electrons was found to decrease slightly as the density of the dots increases from 1.2 to 3×10^9 dots cm^{-2}. Our study reveals that inter-dot tunnelling coupled with Coulombic interaction between the dots and the charged traps in the plane containing the QDs was found to significantly affect the charge trapping ability of the QDs.

(Some figures in this article are in colour only in the electronic version)

Memory devices based on semiconductor quantum dots (QDs) provide a promising future option for ultra-high density memory devices [1–3]. The storage capacity of memory devices based on QDs is expected to approach a 1 Tbit in^{-2} storage density in the near future [4]. In order to achieve this expected storage density; there are several challenges that need to be addressed. Controlling the size and distribution of QDs, increasing the memory storage period (which is currently in weeks) and achieving a reliable room temperature operation are some of the outstanding issues which have to be solved before the commercialization of QD based memory devices [5–7]. Already some experimental techniques have been developed to achieve uniformity in the density and the size distribution of QDs [8, 9]. Some major progress has also been made towards improving the performance of the QD devices at room temperature [10, 11]. Notwithstanding the progress made so far, the reliable trapping of electrons in the QDs rather than in the deep level defect centres still remains very challenging [7, 12].

In highly dense QD memory devices the aerial density of the QDs will be around 10^{11} dots cm^{-2}. Since the QDs are formed by strain relaxation, a considerable number of strain induced defect centres will be formed around the vicinity of the dots [13]. Theoretically it is predicted that the inter-dot electron tunnelling and the Coulombic interaction between the electrons in the nearby dots become stronger when large numbers of dots are confined to a small area [14]. Therefore inter-dot Coulombic interactions and the presence of defect centres may significantly limit the storage capacity of the memory device. For successful realization of ultra-high density QD memory devices, the effect of these factors on the charge trapping ability of the QDs had to be investigated. So far, few experimental efforts had been undertaken to investigate this phenomenon. In this study, the correlation between the density and electron trapping ability of the QDs was investigated. Three QD samples with different dot densities were chosen and their memory characteristics such as charge storage density and retention time were studied. The study was carried out by taking capacitance–voltage (C–V) and current–voltage (I–V) measurements at different temperatures.

The sample used for this study was a GaAs/AlGaAs single quantum well structure grown by molecular beam epitaxy. The heterostructure was grown on the GaAs substrate and consisted of a 20 nm wide GaAs/$Al_{0.33}Ga_{0.67}As$ quantum well that was embedded with InAs QDs at the centre of the quantum well (figure 1) [15]. Silicon was doped at a concentration of 1.1 E18 cm^{-3} in the 40 nm AlGaAs layer, which was separated from the quantum well by a 40 nm AlGaAs barrier. Hall bars of

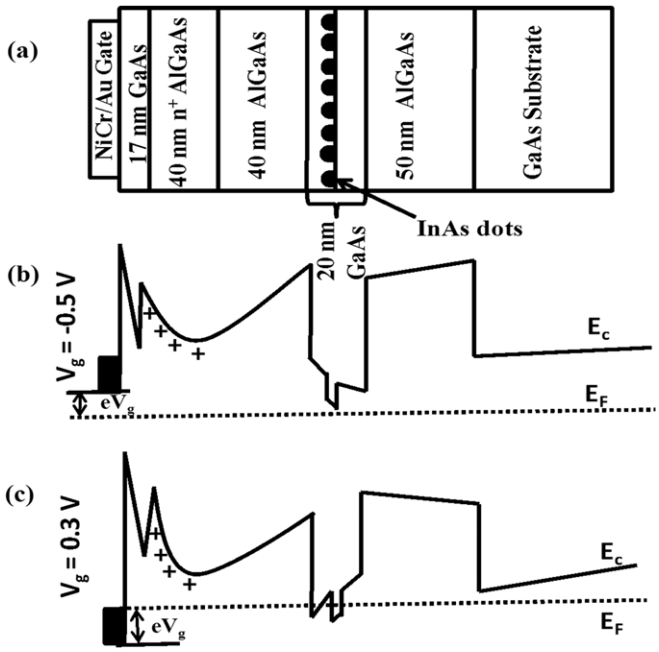

Figure 1. Schematics of the sample structure of the QD device. Conduction band diagram of the device at (*b*) $V_g = -0.5$ V and (*c*) $V_g = 0.3$ V.

length 800 μm and width 80 μm were fabricated using standard photolithographic techniques. A NiCr/Au gate was deposited to form a surface Schottky gate.

The three QD devices (C1335c, C1335m, C1335e) employed in this study were fabricated from the centre, middle (midway between the centre and the edge of the wafer) and edge of the wafer, respectively. The device fabricated at the centre of the wafer has higher dot densities as compared with the ones derived from the middle and the edge regions due to the relative differences in the InAs flux rate. The dot densities in our samples vary from 1.2×10^9 to 3×10^9 cm^{-2}, from the edge to the centre of the wafer [16]. The error in the estimation of dot density is approximately 6.4%, which is the maximum difference found between the density distribution on the same sample counting from an area of 12 μm^{-2}. From the high resolution TEM image, the height and width of the dots were found to be 4 nm and 28 nm, respectively ((sample 2) in [14]) [17]. We observed 13% variation in the size distribution of the QDs for the device under study. Due to the narrow size distribution of the QDs, our heterostructure is ideally suited for studying the charge storage mechanism in the dots.

The sample was then loaded into a closed cycle cryostat to perform the I–V and C–V measurements. C–V measurements were taken using a Keithley 4200 semiconductor characterization system by connecting the sensing terminal to the Ohmic and the signal [ac(20 mV$_{rms}$) + dc] terminal to the gate (figure 2). For the I–V measurements a three terminal configuration was employed. A constant dc bias of 0.1 V was applied between the two ohmic contacts and the variations in the drain current were recorded as a function of the gate voltage. The sweep rate for the gate voltage was maintained at 5 mV s^{-1} for the I–V and C–V measurements. In the C–V measurement, the measurement error is estimated

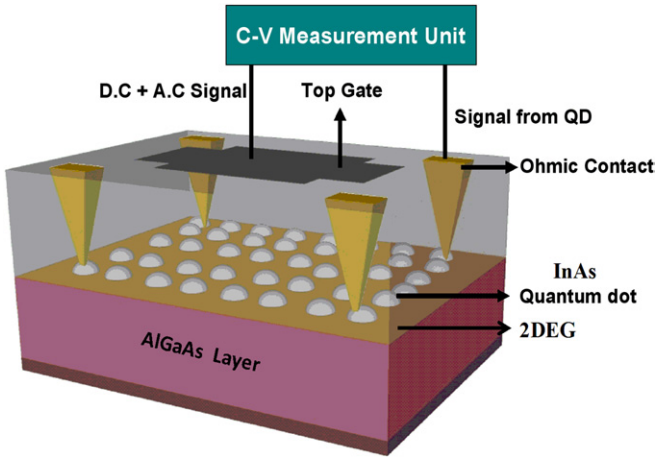

Figure 2. Schematics of the experimental set-up used for taking the C–V measurements.

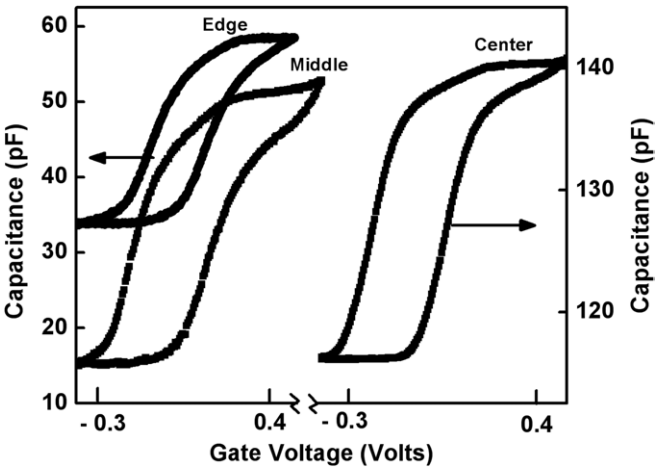

Figure 3. Capacitance–voltage characteristics of the QD samples derived from the centre, middle and the edge of the wafer at 100 K. The measurement frequency is 100 kHz.

to be approximately less than 1% at a gate bias of ± 0.5 V by taking into account the effects of gate tunnelling current and channel resistance.

Figure 3 shows the C–V characteristics of all three QD samples. The clockwise hysteresis loop observed in the C–V traces as the gate bias (V_g) was ramped cyclically, is a clear signature of electrons being trapped in the QDs. The capacitance response from the heterostructures with embedded QDs is a combination of the capacitance of the QDs in series with the resistance of the 2DEG. A larger capacitance corresponds to a state in which the dots are populated with electrons ('1') and the smaller capacitance represents a '0' in which the dots are empty of electrons. The sharp increase (decrease) in capacitance observed during the forward (reverse) sweep is due to the gradual increase (decrease) in the 2DEG density in the quantum well. From the hysteresis curve, the number of electrons that are trapped in the QDs can be calculated from the difference in the capacitance values at zero bias. The number of electrons trapped in the QDs can be determined from the formula [18]

$$n_{qd} = (C_F - C_R) \times \Delta V / eA, \quad (1)$$

Table 1. Comparison between capacitance values of edge, middle and centre samples.

Sample name	Capacitance at '1' state (pF)	Capacitance at '0' state (pF)	Geometric capacitance (pF)	Hysteresis width (V)
Edge	58	34	54.67	0.20
Middle	51.5	15.7	54.67	0.30
Centre	140	115	54.67	0.27

where n_{qd} is the number of electrons in the QD, $C_{F,R}$ is the value of the capacitance at the zero bias during the forward and reverse sweep, e is the electronic charge, A is the area of the Hall bar and ΔV is the hysteresis width. From the C–V characteristics of figure 3, the numbers of trapped electrons are found to be 1.27×10^7, 3.17×10^7 and 1.32×10^7 electrons cm^{-2} in the edge, middle and centre samples, respectively. The densities of the dots being on the order of $10^9\,cm^{-2}$, it is clear that not all the dots contain electrons. Another striking observation is that the storage density (the number of trapped electrons/unit area) for the centre sample whose dot density is the highest is less as compared with the middle one. This result indicates that the storage density of the QD device is not always directly related to the density of the dots.

To gain insight into this phenomenon, comparisons were made between the various capacitance values for all three devices. The values are shown in table 1. The geometric capacitance is calculated by modelling the gate and the 2DEG in the quantum well as two parallel plates of a capacitor [12] with a dielectric layer of GaAs and AlGaAs in between. The geometric capacitance (C) is calculated using the formula

$$C = \frac{(2\varepsilon A)}{d}\frac{k_1 k_2}{k_1 + k_2}, \qquad (2)$$

where ε is the permittivity of free space, A is the area of the gate ($800 \times 80\,\mu m^2$), d is the distance between the 2DEG and the gate (117 nm), k_1 is the dielectric constant of GaAs and k_2 is the dielectric constant of AlGaAs. It is well known that in QD devices, additional energy levels are inherently present between the valence and the conduction band which act as electron traps [19, 20]. These additional charge traps contribute to the overall capacitance of the device. The resultant device capacitance will now be a parallel combination of the capacitance of the QDs and the traps. In the absence of any trapped charges in the traps, the capacitance of the device should be approximately equal to the geometric capacitance at the saturation regime ('1' state) when the 2DEG and QDs have a maximum number of electrons [21]. In the middle and the edge samples, the capacitance at the '1' state was almost equal to the geometric capacitance. This shows that even though the traps are present in the edge and middle samples, their presence seems to have very little effect on the overall capacitance. This might be due to the low concentration of strain induced defects. However, in the centre sample, the saturation capacitance was almost three times higher than the geometric capacitance. This is an indication that some of the electrons from the 2DEG may have been captured by the traps present in the vicinity of the dots. In that case, the charged traps contribute to the capacitance response and so the device capacitance will now be significantly increased. Apart from this, the charge traps will enhance the Coulombic interaction and the short range scattering effects. As a result, the probability of the electrons getting trapped in the QDs gets reduced in the centre sample when compared with the other two [12].

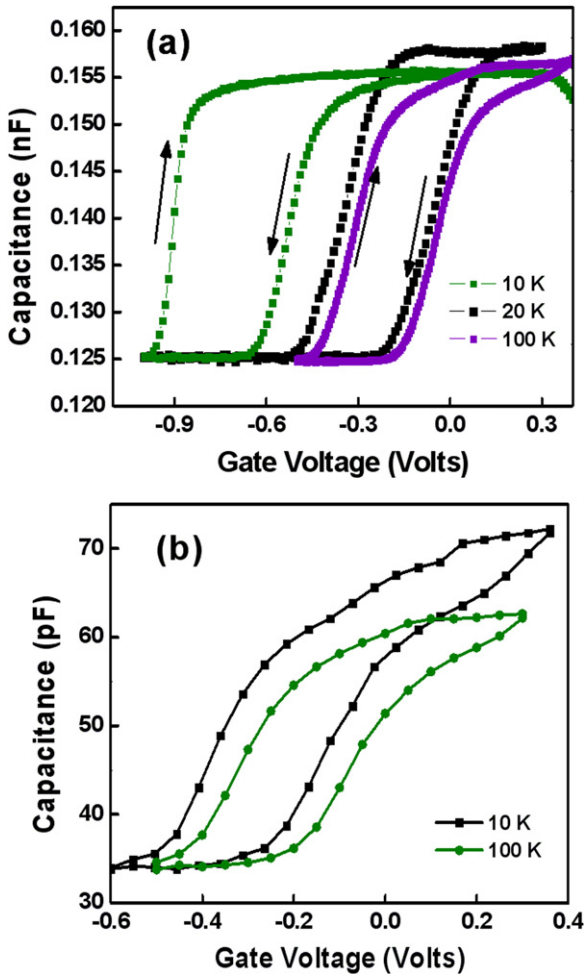

Figure 4. C–V characteristics of the (a) centre and (b) edge samples at different temperatures.

To support our conjecture that the traps are more active in the centre sample and not so in the other two samples, we carried out capacitance–voltage (C–V) measurement for the centre and edge samples at different temperatures and the results are shown in figure 4.

The centre sample was cooled to a temperature of 10 K and a voltage pulse of −1 V was applied for a few seconds to completely deplete the electrons in the QDs and the quantum well. At $V_g = -1$ V, all electronic states of InAs QDs and GaAs quantum well will be raised above the Fermi level and are therefore fully discharged. Only the trap levels associated with the QD layer will lie below the Fermi energy. At low temperatures the charge trapping ability of these traps increases. As the gate bias is gradually increased from −1 V, the capacitance of the sample rapidly increases due to the filling of trap levels and saturates at a gate bias of −0.8 V. Further ramping the gate bias to 0.4 V produced no change

in the capacitance value as the Fermi level is likely to be pinned at the trap states. When the gate bias was reverse swept, no appreciable change in the capacitance value was observed until $V_g = -0.2$ V. Thereafter the capacitance value rapidly decreases, as the electrons start to escape from the traps when their energy levels are brought close to the Fermi energy. It is to be noted that the entire hysteresis loop was observed only in the negative voltage regime, which is a clear indication that the hysteresis behaviour observed at 10 K is due to the traps. C–V sweep is then repeated at 20 and 100 K. The entire hysteresis loop shifted approximately by 0.5 V and the characteristics of the trace resembles that of the conventional QD memory devices where the charge storage occurs in the positive gate voltage regime and normal hysteresis behaviour was observed in the C–V trace. Similar measurements carried out for the edge sample shows no significant difference between the hysteresis curves at 10 and 100 K, which confirms our speculation that the traps in the edge sample are not very active. The same results were observed for the middle sample as well. The following are the inferences that can be made out of this observation.

(1) The disappearance of trap related hysteresis at 20 K indicates that the traps contributing to hysteresis are present in the vicinity of the dots. Previous experimental work also supports our conclusion that the traps related to point defects are more likely to exist in regions where the dot density is the highest [21].
(2) The identical value of the forward and reverse capacitance at $V_g = 0$ V observed in the centre sample at 10 K indicates that the electrons from the 2DEG did not tunnel into the QDs in the positive gate voltage regime. It is a clear indication that when the traps are charged, it significantly affects the charge trapping ability of the QDs. This observation supports our earlier statement that the storage density of the centre sample is affected by the charged traps related to the point defects and strain relaxation. Identical hysteresis behaviour of the edge and middle samples at 10 and 100 K confirms that the role of traps in the low density samples is minimal.

To explain the very low trapping density ($\sim 10^7$ electrons cm^{-2}) in heterostructures with QDs embedded in the quantum well, we employed the theoretical model proposed by Prada and Harrison [14]. According to this model, the charge trapping ability of the QDs depends on four important parameters, namely (a) single particle energy level of the individual QDs, (b) onsite Coulomb interaction, i.e. the repulsive force an electron experiences when it tries to enter into the dots, (c) Coulomb repulsion between electrons in the neighbouring dots and (d) the electron tunnelling process between the dots. The first two parameters which critically depend on the dot size distribution can be neglected due to the fact that the QDs in the devices under study have a narrow size distribution. Only the inter-dot Coulomb interaction and electron tunnelling will have some effect on the charge trapping ability of the QDs. The QDs embedded in the centre sample (which has the highest density) will experience strong inter-dot Coulomb and electron tunnel interactions in comparison with the middle and edge samples. Therefore

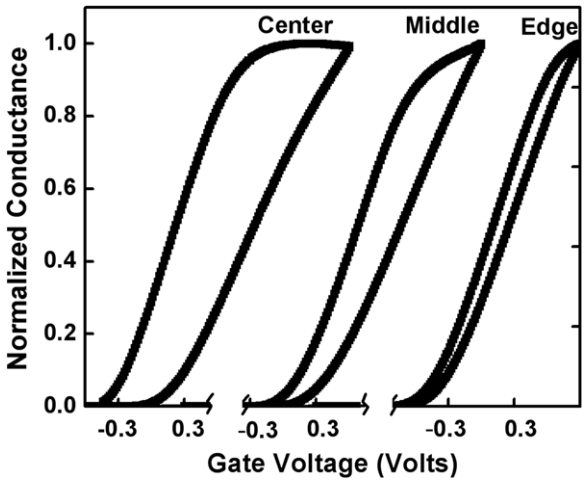

Figure 5. Clockwise hysteresis loop in the conductance measurement for the centre, middle and the edge samples at 100 K. Source drain bias is 100 mV.

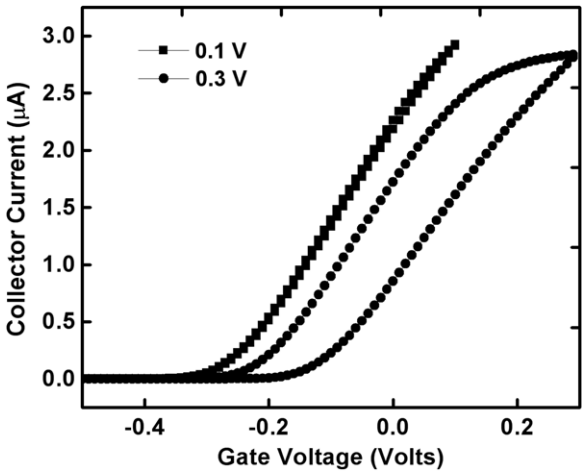

Figure 6. Clockwise hysteresis loop observed in the conductance trace of the centre sample for $V_{gmax} = 0.1$ V and 0.3 V. The source drain bias is fixed at 100 mV.

in the samples with high dot density, the combined effect of these two phenomena will considerably affect the number of electrons that can be stored in the individual QDs. During the writing operation (forward sweep), when the charges begin to accumulate in the QDs, the Coulombic interaction between the dots increases significantly. Since the QDs were embedded in the quantum well, the electrons in the 2DEG will further enhance the lateral inter-dot coupling. Therefore the dots which trap electrons first exert a Coulombic repulsive force on the electrons entering into the neighbouring dots and as a result the overall trapping density is much lower than the QD density in our devices.

The memory operation of all three devices was also demonstrated in the conductance measurement by repeating the aforementioned gate voltage sweep (figure 5). When V_g reaches a positive value, the potential at the QD layer is lowered. The dots and the traps are charged by the electrons from the 2DEG. The reduced 2DEG density results in a lower conductance when V_g is swept in the reverse direction. Apart

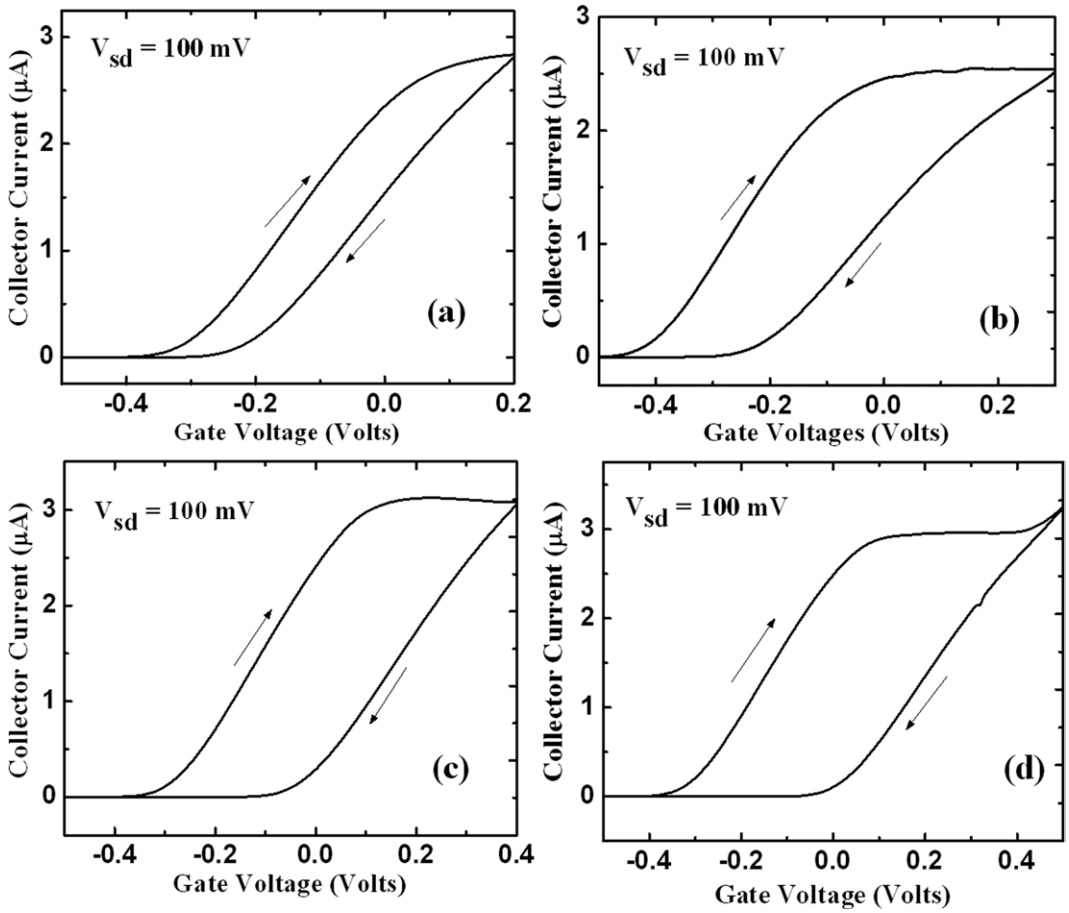

Figure 7. Hysteresis characteristics of the centre sample in the conductance measurement is plotted for different maximum positive gate voltages (*a*) $V_{\mathrm{gmax}} = 0.2$ V, (*b*) $V_{\mathrm{gmax}} = 0.3$ V, (*c*) $V_{\mathrm{gmax}} = 0.4$ V, (*d*) $V_{\mathrm{gmax}} = 0.5$ V.

from this, the charged dots and the traps scatter the 2DEG by Coulombic interactions leading to a further decrease in the 2DEG conductance. Therefore the hysteresis width in the conductance trace was expected to increase with an increase in the dot density. This expected behaviour can be clearly seen in figure 5 in which the area of hysteresis increased proportionally with the dot density (from the edge towards the centre). The hysteresis measurement was then repeated for the centre sample by changing the maximum gate voltage ($V_{\mathrm{g\,max}}$) to which the sweep was then returned. For different $V_{\mathrm{g\,max}}$ the corresponding change in the hysteresis behaviour in the conductance trace was observed.

No hysteresis was observed when the sweeping voltage was limited to 0.1 $V_{\mathrm{g\,max}}$ (figure 6). Hysteresis was observed when $V_{\mathrm{g\,max}}$ was increased above this threshold limit. This indicates that the charge trapping in the QDs occurs only when the gate voltage is increased above 0.1 V. The study was then carried out for $V_{\mathrm{g\,max}} = 0.2$, 0.3, 0.4 and 0.5 V and the results are shown in figure 7. On incrementing the range of $V_{\mathrm{g\,max}}$, the area of the hysteresis loop increased proportionally (figure 7). Since the area enclosed by the hysteresis loop is directly related to the number of electrons trapped by the QDs, the density of the 2DEG will be decreased with an increase in $V_{\mathrm{g\,max}}$. Therefore the threshold voltage required to completely deplete the 2DEG while reverse sweeping the gate decreases with an increase in $V_{\mathrm{g\,max}}$ (figure 7). No significant change was observed in the threshold voltage required to populate the 2DEG during the forward sweep. In the case of middle and edge samples similar characteristics were observed, the difference being in the magnitude of the threshold voltages.

The charge retention times in all three devices were studied by carrying out the real time measurement of the collector current as the gate bias was switched between −0.5 and 0.3 V (erase/write pulse) (figure 8). The electrons were first discharged from the QDs by applying a negative pulse of −0.5 V. A write voltage pulse of 0.3 V is then applied for a few seconds and the change in the collector current was monitored as a function of time under the zero bias condition. As shown in figure 8, the collector current in the device remained stable at 1.9 μA, which is the value of the current observed at $V_{\mathrm{g}} = 0$ after the QDs are saturated with electrons. During the hold period the collector current did not increase, which is an indication that the electrons are not discharged from the QDs. This is in agreement with the theoretically predicted value for the memory devices based on InAs QDs [6]. Similar characteristics were observed for the middle and the edge samples as well.

In conclusion, we investigated the charge trapping ability of the QD memory devices with different dot densities. A clockwise hysteresis loop was observed in the C–V and I–V measurements, which were an indication that the electrons were preferentially trapped in the QDs. The trapping

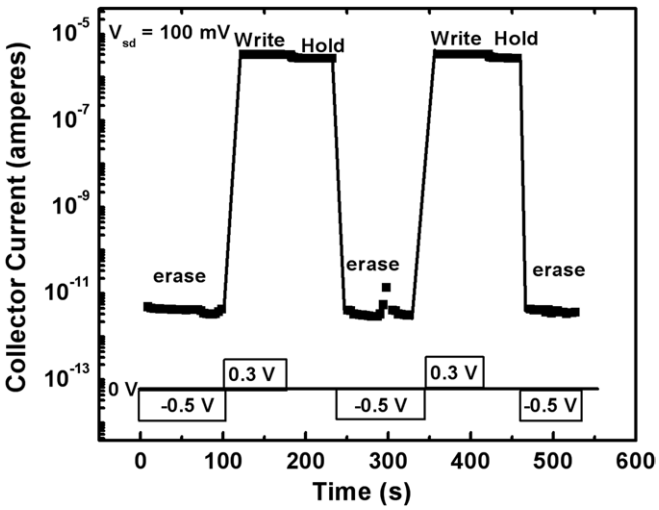

Figure 8. Real time measurement of collector current in the centre sample on applying write/erase pulse through the gate. The source drain bias is maintained at 100 mV.

density calculated from the difference in the capacitance measurements revealed that the number of stored electrons decreases for the centre sample due to the dominating effect of the traps. In the case of the middle and edge sample, the effects of traps are minimal and the electrons are favourably trapped in the QDs. Therefore to achieve a very high storage density in QD memory device, the influence of traps must be given serious consideration and their effect should be minimized by devising a suitable strategy. Even though the heterostructures with embedded QDs have limited storage density, they have an advantage in that the entire memory operation can be carried out by applying a voltage on the order of a few hundred millivolts. Positioning the QDs in the larger band gap region like AlGaAs will increase the charge storage density of the dots as the confinement potential of the electrons in the dots will be higher. However, the devices based on this model need a higher operating voltage and their performances were considerably limited by the presence of deep level defects related to AlGaAs and QD layers. Therefore our proposed device holds great potential towards fabricating low power electrically driven memory device; however, its charge storage density has to be significantly improved to make the device commercially viable.

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